How to Generate a 1.544MHz (or 2.048MHz) Clock Signal from an 8kHz Reference Clock

EXAR

The XRT8000 device can be configured to generate either a T1 (1.544MHz) or E1 (2.048MHz) rate clock signal, from a "Reference Clock signal of frequency 8kHz. The approach that one should use to accomplish all of this is presented below.

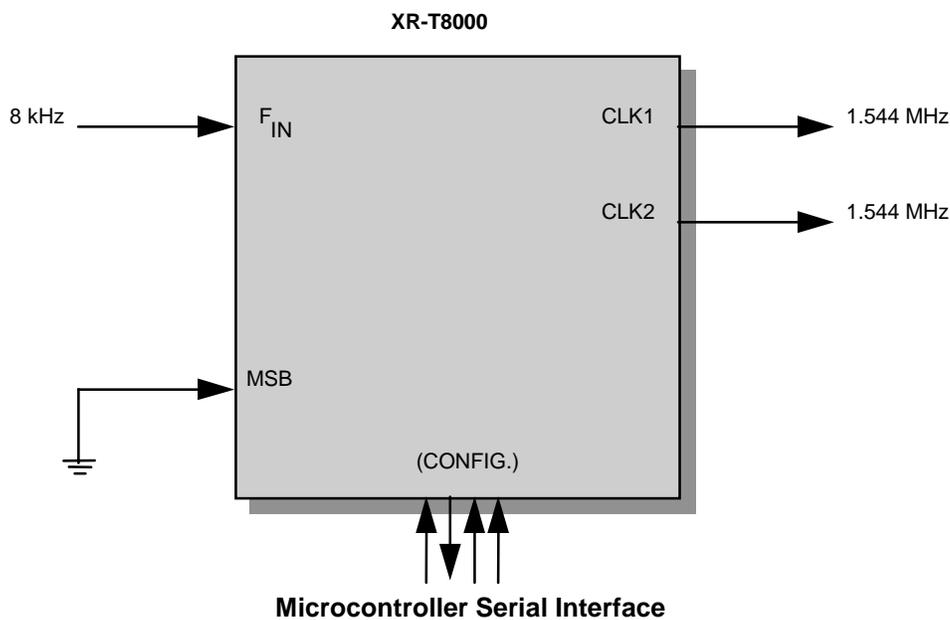1. To generate a 1.544MHz clock signal, from an 8kHz clock signal:

XR-T8000

8 kHz → F_{IN} CLK1 → 1.544 MHz

CLK2 → 1.544 MHz

MSB

(CONFIG.)

Microcontroller Serial Interface

Figure 1. Illustration of the XRT8000 device generating a 1.544MHz clock signal from an 8kHz Reference clock signal (Reverse/Slave Mode).

In order to configure the XRT8000 device to operate in this manner, the user must configure the chip to operate in the "Reverse/Slave" Mode. The user accomplishes this by executing the following steps:

   Pull the MSB pin (pin 8) "low".

This will configure the device to operate in the "Slave" Mode.

   Write the following values, into the corresponding "Configuration Registers", (via the Microprocessor Serial Interface) as tabulated below in Table 1.

Step Number	Configuration Register	Value (to be written)	Comments
1	CR1	01101	The first four bits (e.g., "0110") configures the chip to operate in the "Reverse" Mode. Further, it configures each of the PLLs to generate a 1.544 MHz clock signal. Setting the fifth bit to "1", enables PLL #1. If one does not wish to generate the 1.544 MHz clock via pin 6, then one should set this bit to "0".
2	CR2	00001	This step simply enables PLL #2 to output a 1.544 MHz clock via the "CLK2" output pin (pin 13). If one does not wish to output any signal via this pin, then he/she should write "00000" to this register.
3	CR3	xxxxx	This step can be skipped
4	CR4	xxxxx	This step can be skipped
5	CR5	11100	This step enables the XRT8000 to output the 8kHz output via the SYNC output pin (pin 2), and the PLL_1 and PLL_2 outputs via the CLK1 (pin 6) and CLK2 (pin 13) output pins, respectively.

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Table 1. Programming Procedure, via the Microprocessor Serial Interface

By executing the above-mentioned procedure, the XRT8000 device will be configured to operate in the "Forward/Slave" Mode, and will generate a 2.048MHz clock via the CLK1 and CLK2 output pins, when receiving an 8kHz signal at the F_{IN} input pin (pin 3).

2. To generate a 2.048MHz clock signal, from an 8kHz clock signal:

XR-T8000

8 kHz ——————▶ F IN   CLK1 ————▶ 2.048 MHz

                                CLK2 ————▶ 2.048 MHz

————————▶ MSB

           (CONFIG.)
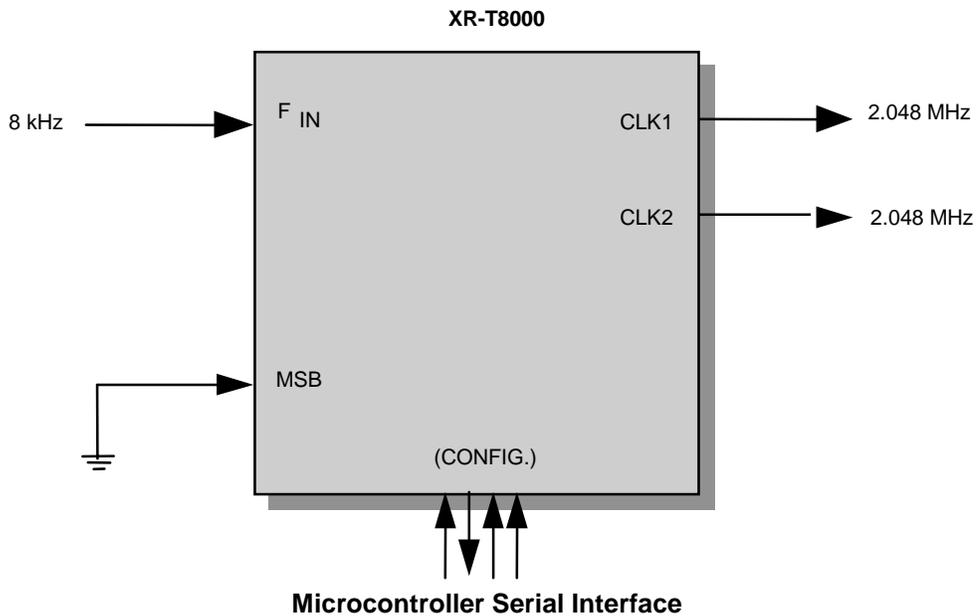
Microcontroller Serial Interface

**Figure 2. Illustration of the XRT8000 device generating a
2.048MHz clock signal from an 8 kHz Reference clock signal (Reverse/Slave Mode).**

In order to configure the XRT8000 device to operate in this manner, the user must config-
ure the chip to operate in the "Forward/Slave" Mode. This user accomplishes this by
executing the following steps:

   Pull the MSB pin (pin 8) "low".

This will configure the device to operate in the "Slave" Mode.

   *Write the following values, into the corresponding "Configuration Registers",
   (via the Microprocessor Serial Interface) as tabulated below.*

Step Number	Configuration Register	Value (to be written)	Comments
1	CR1	00101	The first four bits (e.g., "0010") figures the chip to operate in the "Forward" Mode. Further, it configures each PLL to generate a "k x 64" clock signal. **Note:** The value for "k" is specified in Step # 3. Setting the fifth bit to "1", enables PLL # 1. If one does not wish to generate the 2.048 MHz clock via pin 6, then one should set this bit to "0".
2	CR2	00001	This step simply enables PLL #2 to output a 2.048 MHz clock via the "CLK2" output pin (pin 13). If one does not wish to output any signal via this pin, then he/she should write "00000" to this register.
3	CR3	11111	This step sets the value for "k" for PLL # 1 (see "Comments" for "Step 1") to 32. Consequently, the XRT8000 will generate a clock signal of 2.048 MHz.
4	CR4	11111	This step sets the value for "k" for PLL # 2 (see "Comments" for "Step 1") to 32.
5	CR5	11100	This step enables the XRT8000 to output the 8kH output via the SYNC output pin (pin 2), and the PLL_1 and PLL_2 outputs via the CLK1 (pin 6) and CLK2 (pin 13) output pins, respectively. By executing the above-mentioned procedure, the XRT8000 device will be configured to operate in the "Forward/Slave" Mode, and will generate a 2.048 MHz clock via the CLK1 and CLK2 output pins, when receiving an 8 kHz signal at the FIN input pin (pin 3).

Table 2. Programming Procedure, via the Microprocessor Serial Interface

By executing the above-mentioned procedure, the XRT8000 device will be configured to operate in the "Forward/Slave" Mode, and will generate a 2.048 MHz clock via the CLK1 and CLK2 output pins, when receiving an 8 kHz signal at the FIN input pin (pin 3).

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