A Comparision between Exar's XR-88C681 and Motorola's MC2681 DUART Devices.

Introduction

This Applications Note briefly summarizes the differences between the XR-88C681 and the Motorola MC2681 DUART devices.

In general, these two device appear to be very compatible with each other. Their pin outs for both the 44 pin PLCC and 40 pin DIP packages are exactly the same. There are, however, some firmware (programming) differences between the two devices, that must be addressed by the user, if alternate sourcing between these two devices is to be achieved. Some of these differences between the XR-88C681 and the MC2681 are presented below.

1. XR-88C681's Z-Mode

The XR-88C681 allows the user to Command the DUART into the Z-Mode (sometimes referred to as the "Zilog" Mode). This mode can be useful if the user wishes to daisy chain a series of DUART's together, as shown in Figure 1.

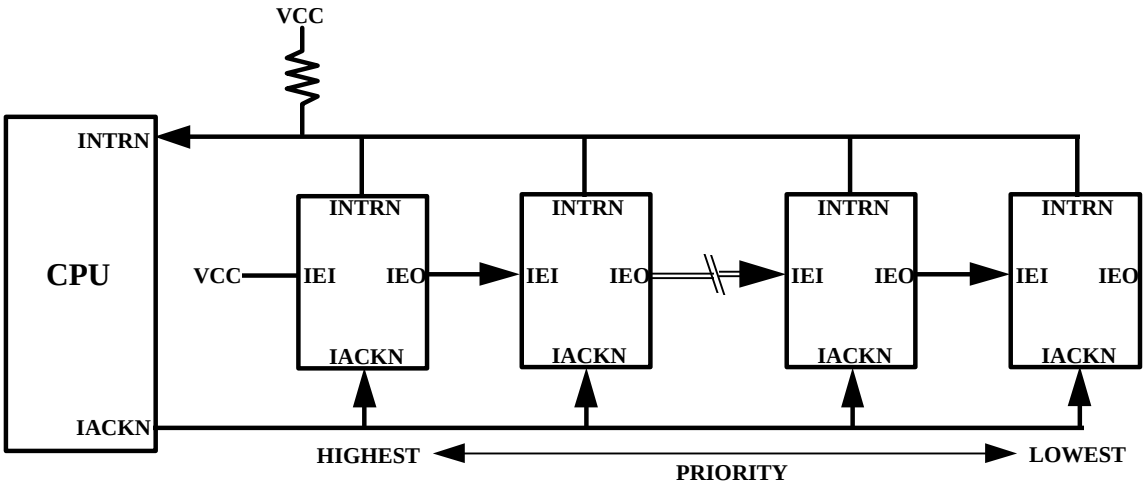

Figure 1, An Illustration of XR-88C681 devices operating in a Daisy Chain, when commanded into the Z-Mode.

A more detailed discussion of the XR-88C681's Z Mode operation can be found in the Data Sheet. However, for the sake of this report, let's just say that the Z-Mode is a manner which allows several DUARTs to be configured in a Daisy Chain, as presented in

Figure 1, and allows the CPU to perform Vectored Interrupt Processing and Interrupt Prioritization for all of the DUART devices.

The MC2681 does not offer the Z-Mode of operation.

2. Register Addressing

Both of these DUARTs contain registers that can be read from or written to. Each of these registers can be accessed by specifying its address via the 4 Address Bit Inputs. This access of the DUART Registers via the Address Inputs is referred to as "Register Addressing".

The Register Addressing between these two devices are slightly difference. Please note that some of these DUART registers are "Read Only" registers, and some are "Write Only" registers. Therefore, the Register Addressing comparison is based on "Read Mode" Register Access and "Write Mode" Register Access. Table 1 presents the DUART Address and the corresponding "Read" mode registers that the will be accessed for each of these two devices.

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Table 1, Register Addressing of "Read Mode" Registers for the XR-88C681 and the MC2681 devices

DUART Address Bits				DUART Device/Read Mode Registers	
A3	**A2**	**A1**	**A0**	**XR-88C681**	**MC2681**
0	0	0	0	Mode Registers, Channel A (MR1A, MR2A)	Mode Registers, Channel A (MR1A, MR2A)
0	0	0	1	Status Register, Channel A, (SRA)	Status Register, Channel A, (SRA)
0	***0***	***1***	***0***	***Masked Interrupt Status Register (MISR)***	***Do not access***
0	0	1	1	Receiver Holding Register, Channel A (RHRA)	Receiver Holding Register, Channel A (RHRA)
0	1	0	0	Input Port Change Register (IPCR)	Input Port Change Register (IPCR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
0	1	1	0	Counter/Timer Upper Byte Register (CTUR)	Counter/Timer Upper Byte Register (CTUR)
0	1	1	1	Counter/Timer Lower Byte Register (CTLR)	Counter/Timer Lower Byte Register (CTLR)
1	0	0	0	Mode Registers, Channel B (MR1B, MR2B)	Mode Registers, Channel B (MR1B, MR2B)
1	0	0	1	Status Register, Channel B (SRB)	Status Register, Channel B (SRB)
1	0	1	0	RESERVED	Do Not Access
1	0	1	1	Receiver Holding Register, Channel B (RHRB)	Receiver Holding Register, Channel B (RHRB)
1	***1***	***0***	***0***	***Interrupt Vector Register***	***Do Not Access***
1	1	0	1	Input Port	Input Port
1	1	1	0	Start Counter Command	Start Counter Command
1	1	1	1	Stop Counter Command	Stop Counter Command

Note: Differences between these two devices are in Bold-Italics
Shaded boxes denote "Address Triggered" Commands

Table 2 presents the DUART Address and the corresponding "Write" mode Register that will be accessed for each of these two devices.

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Table 2, Register Addressing of "Write Mode" Registers for both the XR-88C681 and the MC2681 devices

DUART Address Bits				DUART Devices/Write Mode Registers	
A3	**A2**	**A1**	**A0**	**XR-88C681**	**MC2681**
0	0	0	0	Mode Registers, Channel A (MR1A, MR2A)	Mode Registers, Channel A (MR1A, MR2A)
0	0	0	1	Clock Select Register, Channel A (CSRA)	Clock Select Register, Channel A (CSRA)
0	0	1	0	Command Register, Channel A (CRA)	Command Register, Channel A (CRA)
0	0	1	1	Transmitter Holding Register, Channel A (THRA)	Transmitter Holding Register, Channel A (THRA)
0	1	0	0	Auxiliary Control Register, (ACR)	Auxiliary Control Register, (ACR)
0	1	0	1	Interrupt Mask Register, (IMR)	Interrupt Mask Register, (IMR)
0	1	1	0	Counter/Timer Upper Byte Register (CTUR)	Counter/Timer Upper Byte Register (CTUR)
0	1	1	1	Counter/Timer Lower Byte Register (CTLR)	Counter/Timer Lower Byte Register (CTLR)
1	0	0	0	Mode Registers, Channel B (MR1B, MR2B)	Mode Registers, Channel B (MR1B, MR2B)
1	0	0	1	Clock Select Register, Channel B, (CSRB)	Clock Select Register, Channel B, (CSRB)
1	0	1	0	Command Register, Channel B (CRB)	Command Register, Channel B (CRB)
1	0	1	1	Transmitter Holding Register, Channel B (THRB)	Transmitter Holding Register, Channel B (THRB)
1	***1***	***0***	***0***	***Interrupt Vector Register (IVR)***	***Do Not Access***
1	1	0	1	Output Port Configuration Register (OPCR)	Output Port Configuration Register (OPCR)
1	1	1	0	Set Output Port Bits Command	Set Output Port Bits Command
1	1	1	1	Clear Output Port Bits Command	Clear Output Port Bits Command

Note: Differences between these two devices are in Bold-Italics
Shaded boxes denote "Address Triggered" Commands.

3. Command Register Bit Formats

For both of these DUART devices, each Channel contains an associated Command Register. In general, the Channel Command Register can be written to in order "Enable or Disable the Transmitter and/or Receiver". However, there are numerous "Miscellaneous" Commands which can be invoked by writing to the Channel Command Register.

The Command Register Bit Formats are slightly different between the XR-88C681 and the MC2681 devices. Tables 3 and 4 present a summary of the Bit Formats for the Command Registers, for each of these devices, respectively. Please note that this information applies to both Channels A and B.

Table 3, Bit Format of Command Register (Channels A and B) for the XR-88C681 Device

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Miscellaneous Commands				Transmitter Commands		Receiver Commands	
See Table 5				00 = No Change 01 = Enable Tx 10 = Disable Tx 11 = Do Not Use (Indeterminate)		00 = No Change 01 = Enable Rx 10 = Disable Rx 11 = Do Not Use (Indeterminate)	

Table 4, Bit Format of Command Register (Channels A and B) for the MC2681 Device

Bit 7*	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Miscellaneous Commands			Transmitter Commands		Receiver Commands	
Not Used	See Table 5			00 = No Change 01 = Enable Tx 10 = Disable Tx 11 = Do Not Use (Indeterminate)		00 = No Change 01 = Enable Rx 10 = Disable Rx 11 = Do Not Use (Indeterminate)	

* Bit 7 is not used and may be set to either zero or one.

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Both Tables 3 and 4 call for Table 5 where the Bit Formats for the Miscellaneous Commands are defined for both the XR-88C681 and the MC2681 devices. Please note that the XR-88C681 uses four bits out of the Command Registers for the Miscellaneous Commands; whereas, the MC2681 only uses three bits out of the Command Register. When writing to one of the Command Registers of the MC2681 device, the Most Significant Bit (MSB) is interpreted as a "Don't Care". Consequently only 8 different Miscellaneous Commands are available from the MC2681. In contrast, 14 different Miscellaneous Commands are available with the XR-88C681 device. The commands listed in Table 5 applies to both Channels A and B, unless otherwise specified.

Table 5, Bit Formats for the Miscellaneous Commands (CRn[7:4]) in the Command Registers for both the XR-88C681 and the MC2681 Devices

Bit 7	Bit 6	Bit 5	Bit 4	XR-88C681	MC2681
0	0	0	0	Null Command	Null Command
0	0	0	1	Reset MR Pointer	Reset MR Pointer
0	0	1	0	Reset Receiver	Reset Receiver
0	0	1	1	Reset Transmitter	Reset Transmitter
0	1	0	0	Reset Error Status	Reset Error Status
0	1	0	1	Reset Channel's Break Change Interrupt	Reset Channel's Break Change Interrupt
0	1	1	0	Start Break	Start Break
0	1	1	1	Stop Break	Stop Break
1	***0***	***0***	***0***	***Set Receiver BRG Select Extend Bit***	***Null Command***
1	***0***	***0***	***1***	***Clear Receiver BRG Select Extend Bit***	***Reset MR Pointer***
1	***0***	***1***	***0***	***Set Transmitter BRG Select Extend Bit***	***Reset Receiver***
1	***0***	***1***	***1***	***Clear Transmitter BRG Select Extend Bit***	***Reset Transmitter***
1	***1***	***0***	***0***	***Channel A: Set Standby Mode**** ***Channel B: Reset IUS Latch****	***Reset Error Status***
1	***1***	***0***	***1***	***Channel A: Set Active Mode**** ***Channel B: Set Z-Mode****	***Reset Channel's Break Change Interrupt***
1	***1***	***1***	***0***	***Reserved - do not invoke during operation***	***Start Break***
1	***1***	***1***	***1***	***Reserved - do not invoke during operation***	***Stop Break***

* This is a chip level command (e.g., effects the operation of both channels). Hence this command is invoked only if written to the specified Channel Command Register.

4. Bit Rate Selection

Table 5 presented several Miscellaneous Commands that are available in the XR-88C681 device. However, these commands are not available in the MC2681 device. Some of these commands which effect Bit Rate Selection are presented below:

- Set Receiver BRG Select Extend Bit
- Clear Receiver BRG Select Extend Bit
- Set Transmitter BRG Select Extend Bit
- Clear Transmitter BRG Select Extend Bit

These BRG Select Extend Bits provide additional de-multiplexing of the range of bit rates that are available to the user. Consequently, the XR-88C681 is able to provide the user with 23 different standard bit rates from the Bit Rate Generator portion of the Timing Control Block. In contrast, the MC2681 is able to provide the user with 18 different standard bit rates from the Bit Rate Generator. For more details into the role of the BRG Select Extend Bits, please see the XR-68C681/88C681 Data Sheet.