GENERAL DESCRIPTION

The SP6669 is a synchronous current mode PWM step down (buck) converter capable of delivering up to 800mA of current. It features a pulse skip mode (PSM) for light load efficiency and a LDO mode for 100% duty cycle.

With a 2.5V to 6.0V input voltage range and a 1.5MHz switching frequency, the SP6669 allows the use of small surface mount inductors and capacitors ideal for battery powered portable applications. The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Low output voltages are easily supported with the 0.6V feedback reference voltage.

Built-in over temperature and output over voltage lock-out protections insure safe operations under abnormal operating conditions.

The SP6669 is offered in a RoHS compliant, “green”/halogen free 5-pin SOT23 package.

APPLICATIONS

- Portable Equipment
- Battery Operated Equipment
- Audio-Video Equipment
- Networking & Telecom Equipment

FEATURES

- Guaranteed 800mA Output Current
  - Input Voltage: 2.5V to 6.0V
- 1.5MHz PWM Current Mode Control
  - 100% Duty Cycle LDO Mode Operations
  - Achieves 97% Efficiency
- 0.6V 2% Accurate Reference
- Excellent Line/Load Transient Response
- 18µA Quiescent Current
- Over Temperature Protection
- RoHS Compliant “Green”/Halogen Free 5-Pin SOT23 Package

TYPICAL APPLICATION DIAGRAM

Fig. 1: SP6669 Application Diagram (Adj. version shown)
ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

- Input Voltage \( V_{\text{IN}} \) ....................................... -0.3V to 6.6V
- Enable \( V_{\text{FB}} \) Voltage ....................................... -0.3V to \( V_{\text{IN}} \)
- SW Voltage ...................................... -0.3V to \( (V_{\text{IN}}+0.3V) \)
- Peak Switch Sink/Source Current ............................ 1.3A
- Junction Temperature .......................................... 150°C
- Storage Temperature .............................. -65°C to 150°C
- Lead Temperature (Soldering, 10 sec) ................... 260°C
- ESD Rating (HBM - Human Body Model) ............... 2kV
- ESD Rating (CDM - Charged Device Model) ............ 500V

OPERATING RATINGS

- Input Voltage Range \( V_{\text{IN}} \).................. 2.5V to 6.0V
- Operating Temperature Range...................... -40°C to 85°C
- Operating Junction Temperature \( ^1 \) ..................125°C
- Thermal Resistance \( \theta_{JA} \) .............................. 134.5°C/W
- Thermal Resistance \( \theta_{JC} \) ................................ 81°C/W

Note 1: \( T_J \) is a function of the ambient temperature \( T_A \) and power dissipation \( P_D \) (\( T_J = T_A + P_D \times \theta_{JA} \)).

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of \( T_J = 25°C \) only; limits applying over the full Operating Junction Temperature range are denoted by a “•”. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at \( T_A = 25°C \), and are provided for reference purposes only. Unless otherwise indicated, \( V_{\text{IN}} = 3.6V \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
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<tr>
<td>Feedback Current ( I_{\text{FB}} )</td>
<td>( \pm 30 )</td>
<td>nA</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Regulated Feedback Voltage ( V_{\text{FB}} )</td>
<td>0.588</td>
<td>0.600</td>
<td>0.612</td>
<td>V</td>
<td>•</td>
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<tr>
<td>Reference Voltage Line Regulation ( \Delta V_{\text{FB}} )</td>
<td>0.4</td>
<td>%/V</td>
<td></td>
<td></td>
<td>• ( V_{\text{IN}}=2.5V ) to 5.5V</td>
</tr>
<tr>
<td>Output Over-Voltage Lockout ( \Delta V_{\text{OVL}} )</td>
<td>20</td>
<td>50</td>
<td>80</td>
<td>mV</td>
<td>( \Delta V_{\text{OVL}} = V_{\text{OVL}} - V_{\text{FB}} ) (Adj.)</td>
</tr>
<tr>
<td>Output Voltage Line Regulation ( \Delta V_{\text{OUT}} )</td>
<td>0.6</td>
<td>%/V</td>
<td></td>
<td></td>
<td>• ( V_{\text{IN}}=2.5V ) to 5.5V</td>
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<tr>
<td>Peak Inductor Current ( I_{\text{PK}} )</td>
<td>1.2</td>
<td>2.3</td>
<td>A</td>
<td></td>
<td>( V_{\text{IN}}=3V ), ( V_{\text{FB}}=0.5V )</td>
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<tr>
<td>Output Voltage Load Regulation ( V_{\text{LOADREG}} )</td>
<td>0.5</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Current(^1 ) ( I_{Q} )</td>
<td>18</td>
<td>( \mu A )</td>
<td></td>
<td>( V_{\text{FB}}=0.65V )</td>
<td></td>
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<tr>
<td>Shutdown Current ( I_{\text{SHUTDOWN}} )</td>
<td>0.1</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
<td>( V_{\text{EN}}=0V ), ( V_{\text{IN}}=4.2V )</td>
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<tr>
<td>Oscillator Frequency ( f_{\text{OSC}} )</td>
<td>1.2</td>
<td>1.5</td>
<td>1.8</td>
<td>MHz</td>
<td>• ( V_{\text{FB}}=0.6V )</td>
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<tr>
<td>RDS(ON) of PMOS ( R_{PFEET} )</td>
<td>0.24</td>
<td>( \Omega )</td>
<td></td>
<td></td>
<td>( I_{\text{SW}}=100mA )</td>
</tr>
<tr>
<td>RDS(ON) of NMOS ( R_{NFEET} )</td>
<td>0.24</td>
<td>( \Omega )</td>
<td></td>
<td></td>
<td>( I_{\text{SW}}=100mA )</td>
</tr>
<tr>
<td>SW Leakage ( I_{\text{LSW}} )</td>
<td>( \pm 1 )</td>
<td>( \mu A )</td>
<td></td>
<td></td>
<td>( V_{\text{EN}}=0V ), ( V_{\text{SW}}=0V ) or 5V, ( V_{\text{IN}}=5V )</td>
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<tr>
<td>Enable Threshold ( V_{\text{EN}} )</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td></td>
<td>•</td>
</tr>
<tr>
<td>Shutdown Threshold ( V_{\text{EN}} )</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
<td>•</td>
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<tr>
<td>EN Leakage Current ( I_{\text{EN}} )</td>
<td>( \pm 1 )</td>
<td>( \mu A )</td>
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<td></td>
<td>•</td>
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</table>

Note 1: The dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.
**BLOCK DIAGRAM**

Fig. 2: SP6669 Block Diagram

**PIN ASSIGNMENT**

Fig. 3: SP6669 Pin Assignment
**PIN DESCRIPTION**

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
</table>
| EN   | 1          | Enable Pin. Do not leave the pin floating.  
V<sub>EN</sub>&lt;0.4V: Shutdown mode  
V<sub>EN</sub>&gt;1.2V: Device enabled |
| GND  | 2          | Ground Signal |
| SW   | 3          | Switching Node |
| VIN  | 4          | Power Supply Pin.  
Must be decoupled to ground with a 4.7µF or greater ceramic capacitor. |
| VFB  | 5          | Feedback Input Pin.  
Connect VFB to the center point of the resistor divider. |

**ORDERING INFORMATION**

<table>
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<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Packing Method</th>
<th>Lead-free</th>
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<tbody>
<tr>
<td>SP6669AEK-L/TRR3</td>
<td>-40°C≤T&lt;sub&gt;A&lt;/sub&gt;≤+85°C</td>
<td>SOT23-5</td>
<td>Tape &amp; Reel</td>
<td>Yes</td>
</tr>
<tr>
<td>SP6669EB</td>
<td>SP6669 Evaluation Board</td>
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<td></td>
<td></td>
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</tbody>
</table>

Note: for most up-to-date ordering information and additional information on environmental rating, go to [www.maxlinear.com/SP6669](http://www.maxlinear.com/SP6669)

Note that the SP6669 series is packaged in Tape and Reel with a reverse part orientation as per the following diagram
TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at $V_{IN} = 2.7V$ to 5.5V, $T_J = T_A = 25^\circ C$, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

Fig. 4: Efficiency vs Output Current $V_{OUT} = 1.2V$

Fig. 5: Oscillator Frequency vs. Input Voltage

Fig. 6: EN Pin Threshold vs. Input Voltage

Fig. 7: EN Pin Threshold vs. Temperature

Fig. 8: UVLO Threshold vs. Temperature

Fig. 9: Output Voltage vs Temperature
Fig. 10: Line Regulation

Fig. 11: Load Regulation

Fig. 12: Load Transient Response, I_{out} 250mA to 500mA, V_{out} = 1.2V

Fig. 13: Load Transient Response, I_{out} 10mA to 500mA, V_{out} = 1.2V

Fig. 14: PSM / PWM Boundaries

Fig. 15: Output Voltage Ripple vs Output Current
Fig. 16: Power-ON from EN Pin

Fig. 17: Power-OFF from EN Pin

Fig. 18: PWM Operation

Fig. 19: Short Circuit Response
THEORY OF OPERATION

APPLICATIONS

![Typical Application Circuit](image)

**Fig. 20: Typical Application Circuit**

**INDUCTOR SELECTION**

Inductor ripple current and core saturation are two factors considered to select the inductor value.

\[
\Delta I_L = \frac{1}{f \cdot L} \left( V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \right)
\]

Equation 1 shows the inductor ripple current as a function of the frequency, inductance, \( V_{IN} \) and \( V_{OUT} \). It is recommended to set the ripple current between 30% to 40% of the maximum load current. A low ESR inductor is preferred.

**C\_IN AND C\_OUT SELECTION**

A low ESR input capacitor can prevent large voltage transients at \( V_{IN} \). The RMS current rating of the input capacitor is required to be larger than \( I_{RMS} \) calculated by:

\[
I_{RMS} \approx I_{OMAX} \sqrt{\frac{V_{OUT}^2}{V_{IN}^2} - \frac{(V_{IN} - V_{OUT})}{V_{IN}}}
\]

The ESR rating of the capacitor is an important parameter to select \( C_{OUT} \). The output ripple \( V_{OUT} \) is determined by:

\[
\Delta V_{OUT} \approx \Delta I_L \left( ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right)
\]

Higher values, lower cost ceramic capacitors are now available in smaller sizes. These capacitors have high ripple currents, high voltage ratings and low ESR that makes them ideal for switching regulator applications. As \( C_{OUT} \) does not affect the internal control loop stability, its value can be optimized to balance very low output ripple and circuit size. It is recommended to use an X5R or X7R rated capacitors which have the best temperature and voltage characteristics of all the ceramics for a given value and size.

**SETTING OUTPUT VOLTAGE**

The output voltage is determined by:

\[
V_{OUT} = 0.6 \cdot V \left( 1 + \frac{R_s}{R_i} \right)
\]

**THERMAL CONSIDERATIONS**

Although the SP6669 has an on board over temperature circuitry, the total power dissipation it can support is based on the package thermal capabilities. The formula to ensure safe operation is given in note 1.

**PCB LAYOUT**

The following PCB layout guidelines should be taken into account to ensure proper operation and performance of the SP6669:

1- The GND, SW and \( V_{IN} \) traces should be kept short, direct and wide.

2- \( V_{FB} \) pin must be connected directly to the feedback resistors. The resistor divider network must be connected in parallel to the \( C_{OUT} \) capacitor.

3- The input capacitor \( C_{IN} \) must be kept as close as possible to the \( V_{IN} \) pin.

4- The SW and VFB nodes should be kept as separate as possible to minimize possible effects from the high frequency and voltage swings of the SW node.

5- The ground plates of \( C_{IN} \) and \( C_{OUT} \) should be kept as close as possible.
**OUTPUT VOLTAGE RIPPLE FOR VIN CLOSE TO VOUT**

When the input voltage VIN is close to the output voltage VOUT, the SP6669 transitions smoothly from the switching PWM converter mode into a LDO mode. The following diagram shows the output voltage ripple versus the input voltage for a 3.3V output setting and a 200mA current load.

**DESIGN EXAMPLE**

In a single Lithium-Ion battery powered application, the VIN range is about 2.7V to 4.2V. The desired output voltage is 1.8V.

The inductor value needed can be calculated using the following equation

\[
L = \frac{1}{f \cdot \Delta I} \left( V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \right)
\]

Substituting VOUT=1.8V, VIN=4.2V, ΔIL=180mA to 240mA (30% to 40%) and f=1.3MHz gives

\[
L = 2.86\mu H \text{ to } 3.81\mu H
\]

A 3.3µH inductor can be chosen with this application. An inductor of greater value with less equivalent series resistance would provide better efficiency. The CIN capacitor requires an RMS current rating of at least ILOAD(MAX)/2 and low ESR. In most cases, a ceramic capacitor will satisfy this requirement.
MECHANICAL DIMENSIONS

5-Pin SOT23

Top View

Side View

Front View

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DIMENSIONS IN MM (Control Unit)</th>
<th>DIMENSIONS IN INCH (Reference Unit)</th>
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<tr>
<td>A</td>
<td>MIN: 1.43</td>
<td>MAX: 1.45</td>
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<tr>
<td>A1</td>
<td>0.00</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>0.90</td>
<td>1.15</td>
</tr>
<tr>
<td>b</td>
<td>0.30</td>
<td>0.50</td>
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<tr>
<td>c</td>
<td>0.08</td>
<td>0.22</td>
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<tr>
<td>D</td>
<td>2.90</td>
<td>0.115</td>
</tr>
<tr>
<td>L</td>
<td>2.80</td>
<td>0.111</td>
</tr>
<tr>
<td>E1</td>
<td>1.60</td>
<td>0.063</td>
</tr>
<tr>
<td>e1</td>
<td>0.90</td>
<td>0.036</td>
</tr>
<tr>
<td>L1</td>
<td>0.45</td>
<td>0.018</td>
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<tr>
<td>L2</td>
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<td>0.010</td>
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<tr>
<td>R</td>
<td>0.10</td>
<td>0.004</td>
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<tr>
<td>R1</td>
<td>0.10</td>
<td>0.004</td>
</tr>
<tr>
<td>α</td>
<td>5°</td>
<td>10°</td>
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<tr>
<td>N</td>
<td>5</td>
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Drawing No: P00-00000025
Revision: B
800mA 1.5MHz Synchronous Step Down Converter

REVISION HISTORY

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<th>Date</th>
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<td>2.0.0</td>
<td>07/15/2011</td>
<td>Reformat of datasheet, Updated package specification</td>
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<tr>
<td>2.1.0</td>
<td>02/07/2012</td>
<td>Updated Typical Application schematics and Design example</td>
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<td>2.2.0</td>
<td>11/08/2012</td>
<td>Reformat of datasheet (New logo), Updated Absolute Maximum Ratings, Lead Temperature (Soldering, 10 sec) to 260°C</td>
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<td>2.2.1</td>
<td>05/13/2016</td>
<td>Reformat of datasheet (New logo), Changed oscillator frequency unit</td>
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<td>3.0.0</td>
<td>12/07/2017</td>
<td>Updated I_{OUT}, V_{IN} range, thermal resistance, \Delta V_{OUT}, V_{FB} temperature condition, I_{PK}, I_{Q}, f_{OSC}, R_{DS(ON)}, package drawing (now Mechanical Dimensions), format and Ordering Information. Added PSM and new graphs. Updated to MaxLinear logo. Removed fixed voltage options. New graphs.</td>
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<td>4.0.0</td>
<td>01/07/2020</td>
<td>Updated I_{OUT}, V_{IN} range and V_{IN} absolute max, I_{Q}, I_{PK}, R_{DS(ON)}, Updated graphs. Updated ESD rating.</td>
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<td>07/26/2021</td>
<td>Updated I_{OUT}, V_{IN} range and V_{IN} absolute max, I_{Q}, I_{PK}, R_{DS(ON)}, Updated graphs. Updated ESD rating. PCN 190111A (Addendum) cancels rev 4.0.0, therefore rev 5.0.0 is the same as rev 3.0.0.</td>
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