An Alternative to POLA™ Modules: PowerBlox™

Introduction

The recent popularity of the point of load alliance products have customers asking for cheaper solutions that are compatible with these designs. Because the design and features were kept simple to allow ease of compatibility between vendors, it is also easy to create a supply yourself that meets the same specifications at a fraction of the cost.

This paper reviews the design implementation of a popular POLA™ part PTH12060W having an input voltage range of 10.8-13.2 volts and an output voltage of 1.8 volts at 10Amps. An explanation of the implementation of each feature is provided and instructions on how to do your own design with design examples are shown.

Features to Implement

To create an IC design using a Sipex PowerBlox™ part all specifications of the POLA™ design must and can be met.

Core performance specifications:	-Input and Output Voltage -Output Current and Current limiting -Line, Load regulation and Transient Response -Efficiency -Output Ripple -Set point tolerance
Additional features:	-Up/Down Margin -Tracking -Enable -Output Sense

Core performance specifications can be handled using our on-line design tool. If your supply requires only the basic performance specs our on-line tool can supply you with a Schematic and Bill of Materials by using this link: http://www.transim.com/sipex/PowerProductsLab . Enter your requirements in the provided fields and receive an instant solution you can also fully simulate on-line.

For this design all of the additional features are required so we will start with a design which meets all of the core performance specifications and then examine how to implement each additional feature.

*POLA is a trademark of the Point Of Load Alliance http://www.polagroup.com/

Core Design

Following design principals outlined in our PowerBlox Evaluation Board Manuals the following power supply was designed. Because it is necessary to adjust the output voltage with the particular resistors outlined by the POLA™ spec, R1 in this design was required to be 10kΩ for reasons we will calculate below. The design specifications that were are shown. The specs meet or beat POLA™ specifications.

Specification	Value	How is specification met
Input Voltage Range	10.8 – 13.2 Volts	- PowerBlox part is capable of operation from 9.6 to 22 Volts. - Loop is designed using worst case highest Vin of 13.2 volts - See Test Results
Set-point Tolerance	+/- 2%	- PowerBlox reference is +/-1% - <1% Resistors should be used to maintain <<2% set-point tolerance
Output Current	10Amps Max	- Output Inductor rated for 50°C rise at 14 Amps - Power Dissipation of solution at 10Amps is 2.6 Watts, - Results show PowerBlox device is dissipating 2Watts at full load. The PowerBlox device is capable of this power dissipation on even a poor heat sinking layout up to 85 degrees with no airflow.
Temperature Variation	+/-1%	- Over line and temperature the PowerBlox reference is 1% (on top of initial tolerance of 1%)
Load Regulation	+/- 12mV	-Guaranteed by design, confirmed with results
Line Regulation	+/- 10mV	-Guaranteed by design, confirmed with results
Total Output Variation	+/- 3%	-Since above specs are met, this will be met
Output Voltage Adjust Range	1.2V – 5.5V	-The PowerBlox device is capable of output voltage from 3.3 to 0.8Volts. -This design examines 1.8Vout, however these output voltages can be obtained
Efficiency	at 8Amps	-87% Minimum at 12Vin 25 degrees, results show 89%
Output Ripple	25mV$_{pp}$	-18.8mV$_{pp}$ reached with measurement on straight supply. (no ripple measurement fixture)
Overcurrent Threshold	20A Max	-Overcurrent threshold is set by looking at the drop across the output inductor.The OCP level as tested was 14Amps maximum.
Transient Response	Recovery in <70uS Deviation 100mV max	-deviation measured at 88mV, recovery <60uS
Switching Frequency	255kHz – 345kHz	- These are the PowerBlox frequency specs
Inhibit	>2.65V ON, <1.9V OFF	- These are the PowerBlox UVin pin specs

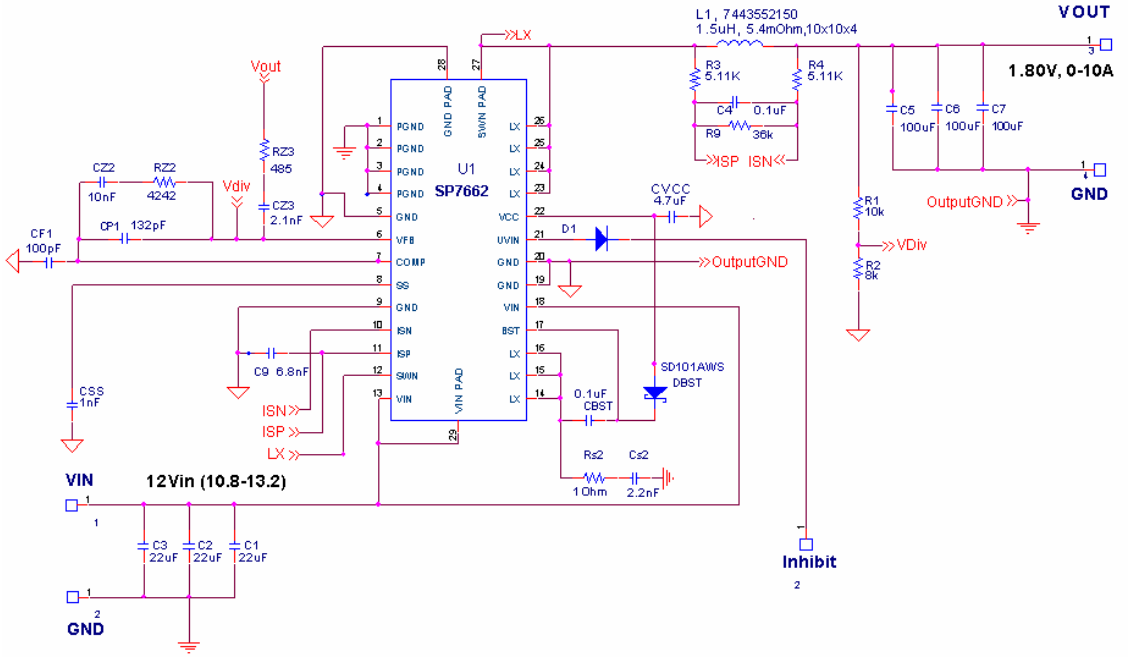


Figure 1 – Core DC-DC Converter Design

Additional Features offered by POLA™ and Implementation

Vout Adjust

By shipping the POLA™ part without a bottom output voltage set-point resistor the user is able to configure the output voltage to levels within a certain range. In the case of the 10A, 12Vin part the low range version is 0.8V to 1.8V. The following equation is used to select the R_{SET} resistor:

$$R_{SET} = 10k\Omega \times \frac{0.8V}{V_o - 0.8V} - 7.87k\Omega \qquad (1)$$

This equation can also be used with the design presented, or you can replace the two set-point resistors with one value.

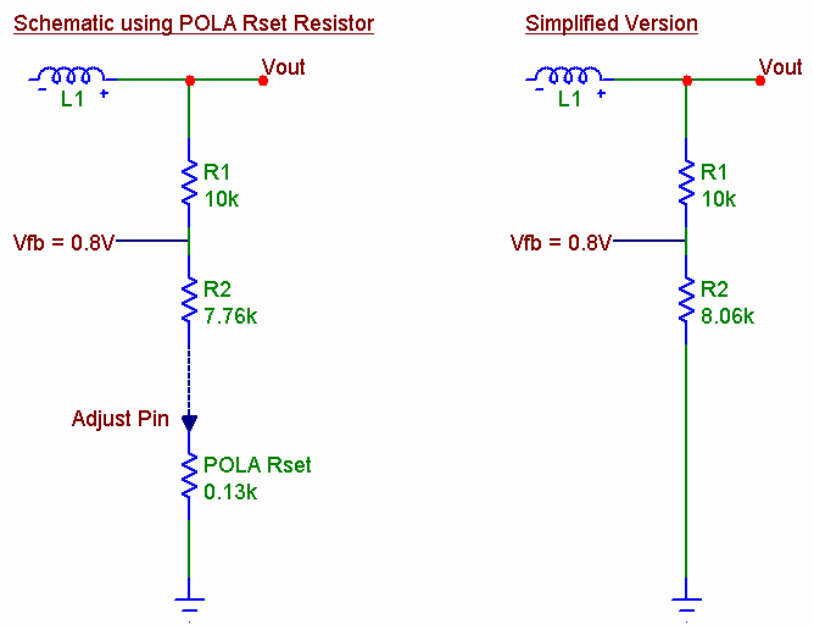


Figure 2 – Setting the Output Voltage

Because the POLA™ part and PowerBlox both use a 0.8V reference configuring the PowerBlox solution to use the same R_{SET} resistor values is very simple. If you are not concerned with using the POLA™ defined R_{SET} resistor values you can use the following equation:

$$R_2 = 10k\Omega \times \frac{0.8V}{V_o - 0.8V} \qquad (2)$$

Place R_2 as shown above in the 'Simplified Version' side of the figure.

Sense

The Output Voltage Sense Feature allows the converter feedback compensation circuitry to see the output voltage directly at the load. The connection between source and load normally has a small value of resistance. For the low power case, it's safe to assume that the DC resistance of the connection between source and load is small enough that its DC effect on the system is negligible. When output current increases and output voltage decrease, the effects of the connection resistance increase proportionally.

For example: take a copper trace 40mils wide X 440 mils long (11mm) of 2 Oz copper – this has a resistance of 2.67mΩ. With 10Amps flowing through it the trace will drop 0.0267 Volts, if not compensated for with a sense connection the output voltage seen by the load would be 1.773 Volts.

Sensing is added by connecting the top of the output voltage set point resistor network directly to the load. Because of the dangerous possibility of this connection becoming open, a Sense Resistor is added between this connection point and the load. The value of 10Ω is selected to minimize the effect on the output voltage set point when sensing is not used.

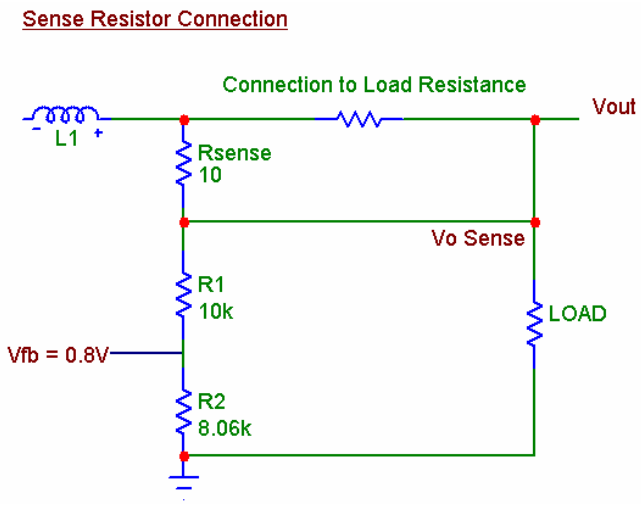


Figure 3 – Placement of Sense Resistor

In short, if you require output voltage sensing, use a 10Ω resistor connected between Vout and R1. Connect to your load at the point between Rsense and R1 (now called $V_O$sense) as close as possible to our load.

If your load is relatively constant and you know the voltage drop seen at your output you can simply permanently increase the converter output voltage by lowering R2. Re-calculate the value using your new required output voltage using the equation 1 or 2 depending on your configuration.

Track

Configuring a PowerBlox part to track the output of another supply is well documented and is one of the prime features of the Power Blox series. A pin called 'Soft Start' is used to implement this feature. The Soft Start pin normally has a capacitor that is charged by a 10uA current source, the voltage on this capacitor controls the speed of the output voltage at turn on.

The Soft Start pin can also be used to override the internal 0.8V reference. If a voltage of 0.8 volts or below is connected, this voltage will be used as the reference. The reference voltage will not be increased beyond 0.8 Volts even if the Soft Start pin voltage is increased to VCC.

By connecting a voltage divider that is equal to the voltage divider used on the output the output voltage can be controlled volt-per-volt. The presence of the 10uA coming from the Soft Start pin will introduce an error in the volt-per-volt control. If using the Track pin to set the steady-state output operating voltage reduce the resistance of R20 and R21 by a factor of 10 or more. This will decrease the error created by the soft start current.

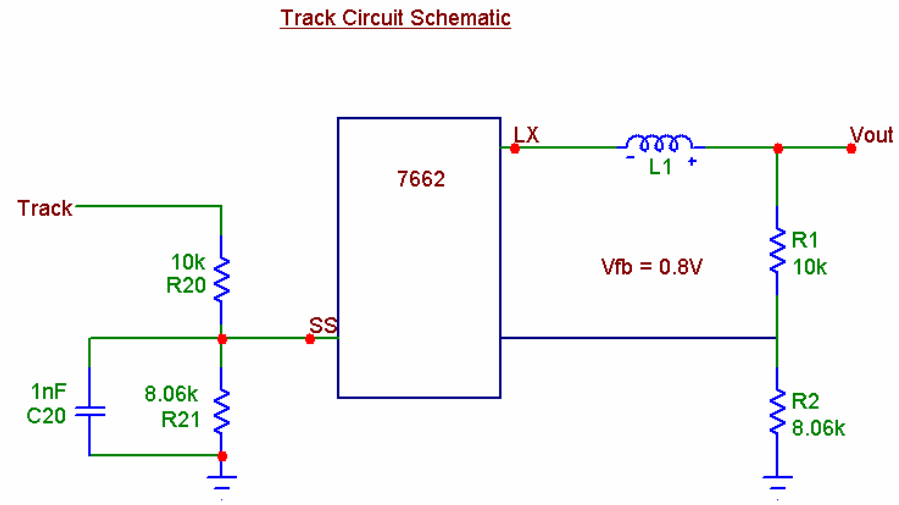


Figure 4 – Track Feature Connection diagram

In the case of this 1.8V converter 10kΩ and 8.06kΩ are used for the output voltage set resistors, so 10kΩ and 8.06kΩ are used for the track set point resistors. Because the voltage at the Soft Start pin will become the new reference, the output will track the voltage seen at the track input on a volt-per-volt basis.

Margin Up / Margin Down

By using external FETs and the Margin Up/Down inputs the converter can be made to run at +5% or -5% of the nominal output set point voltage. This feature is typically used when testing the operation of the circuitry attached to the supply to ensure it will operate within the +/-5% window.

Margin Up

To increase the output of the supply is it necessary to decrease the value of the R_2 resistance as you can see by the following equation:

$$Vout = R1 * \frac{0.8}{R2} + 0.8 \quad (3)$$

To increase the output voltage by 5% we need to reduce the value of R2. We can reduce the value by placing a resistor in parallel with R2. To find this resistor we need to solve the following equation for $R_{M\text{-}UP}$. Where R2 = the parallel combination of R2 and $R_{M\text{-}UP}$.

$$Vout * 1.05 = R1 * \frac{0.8}{((R_{M\text{-}UP} * R_2)/(R_{M\text{-}UP} + R_2))} + 0.8 \quad (4)$$

Where Vout = 1.8 and $R_2 = 8k\Omega$

Here we find $R_{M\text{-}UP}$ to be 88.82kΩ.

This resistor will need to be connected across R_2 using the external FET to margin the part up 5% as shown below.

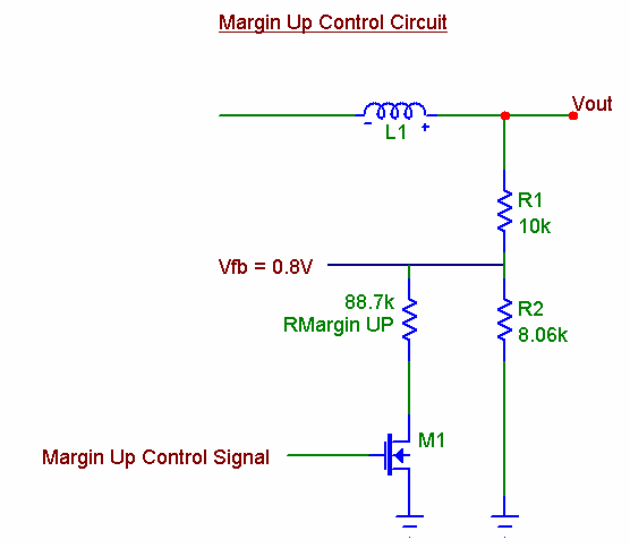


Figure 5 – Margin Up Resistor Connection

Margin Down

To decrease the output of the supply is it necessary to decrease the value of the R_1 resistance, lower the reference voltage, or increase R_2. Reducing R_1 is not practical as this value affects the converter feedback and stability. Decreasing the reference voltage or increasing R_2 are about equal in complexity.

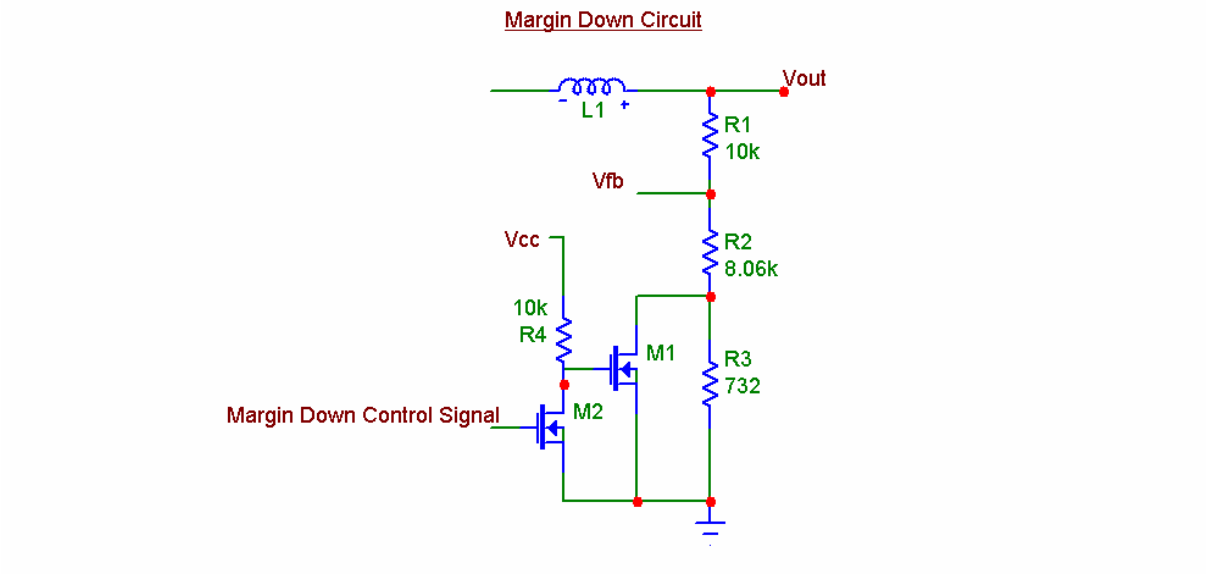


Figure 6 – Margin Down Circuit

The circuit in the figure above uses M1 connected so it is permanently on while the converter is operating, maintaining the nominal output voltage. When it is desired to decrease the output voltage a signal sent to M2 pulls the gate of M1 low shutting the part off and allowing the current to flow through R3 decreasing the current multiplier of R1 and decreasing the output voltage.

Nominal Output Voltage:

$$\text{Vout} = \frac{10k^* 0.8}{8.06k} + 0.8 = 1.793 \ (1.8V) \qquad (5)$$

Margin Down Output Voltage:

$$\text{Vout} = \frac{10k^* 0.8}{(8.06k+732)} + 0.8 = 1.71 \ (1.8V\text{-}5\%) \qquad (6)$$

Any voltage down to the 0.8V reference can be margined using this circuit. Just solve the above equation with the desired output voltage as Vout and solve for the 732 Ohm placeholder.

Final Schematic

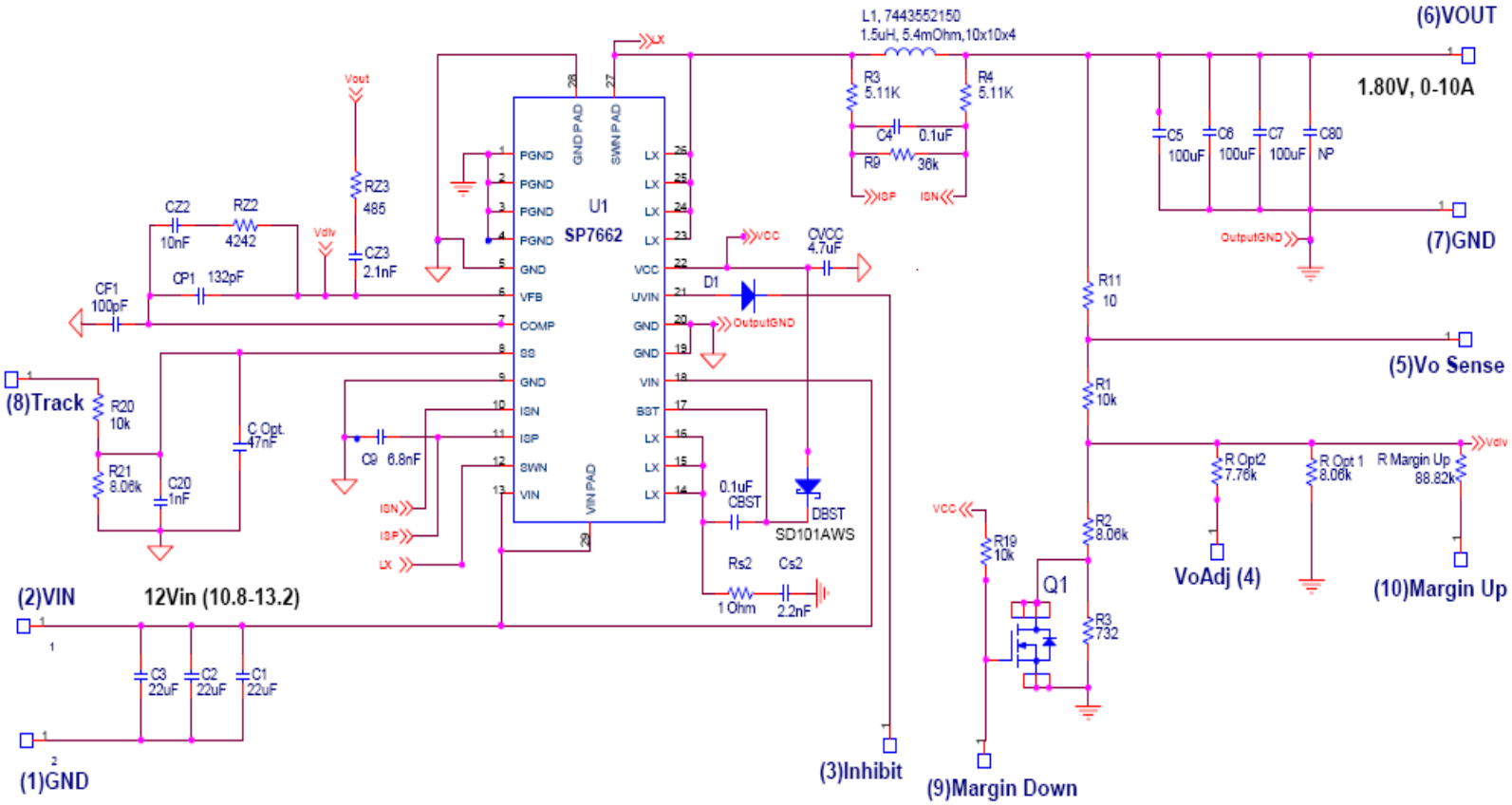


Figure 7 – Final Schematic

A full page version of the schematic is also shown in the appendix. The above schematic shows the implementation of all of the features mentioned in the report. For example 'C Opt' should be used if the Track feature is not being implemented. Use R1, R2, and R3 as shown if the margin down feature is required, etc. If you need assistance configuring the supply contact Sipex Support.

C80 has been left as a placeholder for any additional external capacitance that is required. 300uF of ceramic or 5500uF of non-ceramic having no less than 4mΩ ESR can be used if required. For a fully optimized design for whatever your output capacitance requirements are, please contact Sipex. Because the design is being implemented with discrete components, it is easy to configure the converter feedback loop to obtain the converter performance you require with what ever capacitance you call for.

Design Performance Results:

Efficiency

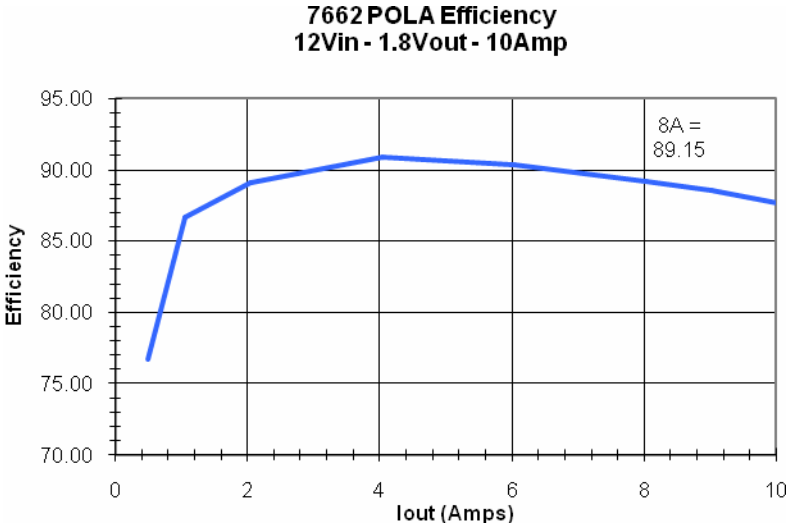


Figure 8 – Design Efficiency (POLA™ quoted efficiency at 8Amp = 87%)

Regulation

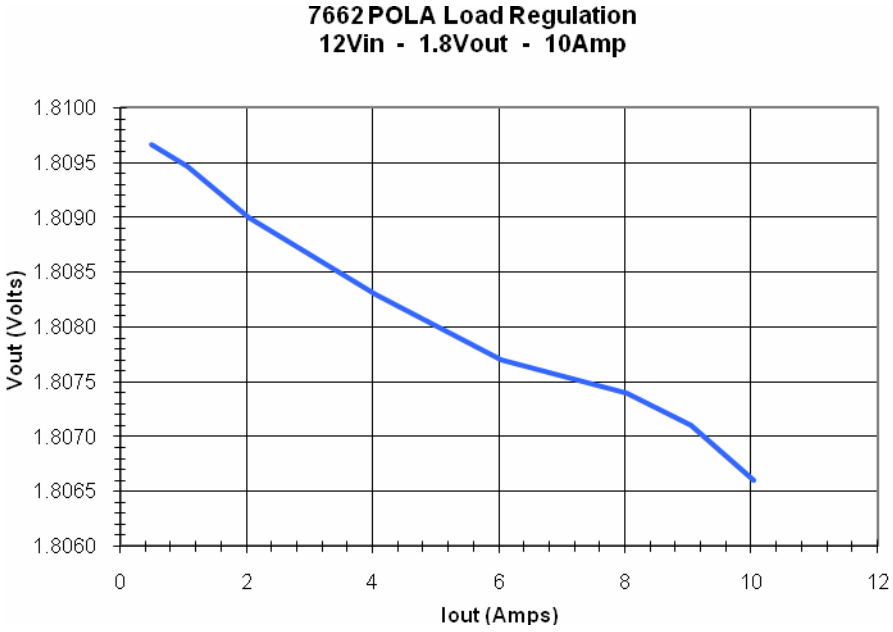


Figure 9 – Solution Regulation (better than POLA™ specifications)

Performance Data

7662 POLA Evaluation Board Test Sheet

Pblox	EVB	Vin	Vo	Io		OCP
7662	7662	10.8-13.2	1.8	10		14A

Vin	Iin	Vout	Iout		Eff	Pout	Pdiss	Pdiss L	Pd PB
12.01	1.72	1.8066	10.03		87.65	18.12	2.55	0.543	2.011
12.01	1.53	1.8071	9.03		88.57	16.32	2.11	0.440	1.666
12.02	1.36	1.8074	8.03		89.15	14.51	1.77	0.348	1.419
12.02	1.01	1.8077	6.04		90.35	10.92	1.17	0.197	0.969
12.03	0.67	1.8083	4.04		90.89	7.31	0.73	0.088	0.644
12.04	0.34	1.8090	2.04		89.10	3.69	0.45	0.022	0.429
12.04	0.18	1.8095	1.05		86.68	1.90	0.29	0.006	0.286
12.04	0.10	1.8097	0.49		76.72	0.89	0.27	0.001	0.268
LoadReg			0.011	%					
			0.0031						

Vin	Iin	Vout	Iout		Eff	Pout	Pdiss	Pdiss L	Pd PB
13.20	1.57	1.8058	10.03		87.40	18.11	2.61	0.543	2.067
13.20	1.40	1.8051	9.03		88.02	16.30	2.22	0.440	1.779
13.21	1.24	1.8051	8.03		88.57	14.49	1.87	0.348	1.522
13.22	0.92	1.8060	6.04		89.81	10.91	1.24	0.197	1.041
13.21	0.61	1.8072	4.04		90.32	7.30	0.78	0.088	0.695
13.22	0.32	1.8082	2.04		88.33	3.69	0.49	0.022	0.465
13.22	0.17	1.8088	1.05		85.51	1.90	0.32	0.006	0.316
13.22	0.09	1.8092	0.49		75.35	0.89	0.29	0.001	0.289
LoadReg			0.025	%					
			0.0041						

Vin	Iin	Vout	Iout		Eff	Pout	Pdiss	Pdiss L	Pd PB
10.81	1.91	1.8052	10.03		87.76	18.11	2.52	0.543	1.981
10.81	1.71	1.8045	9.03		88.34	16.29	2.15	0.440	1.710
10.82	1.50	1.8048	8.03		89.08	14.49	1.78	0.348	1.428
10.81	1.12	1.8058	6.04		90.52	10.91	1.14	0.197	0.946
10.82	0.74	1.8070	4.04		91.33	7.30	0.69	0.088	0.605
10.83	0.38	1.8080	2.04		89.90	3.69	0.41	0.022	0.392
10.81	0.20	1.8081	1.05		87.82	1.90	0.26	0.006	0.257
10.81	0.11	1.8092	0.49		78.10	0.89	0.25	0.001	0.247
LoadReg			0.061	%					
			0.0047						
Line and Load Regulation MAX			0.0052						

Maximum output voltage variation over line and load as noted 5.2mV at 25 degrees Celsius.

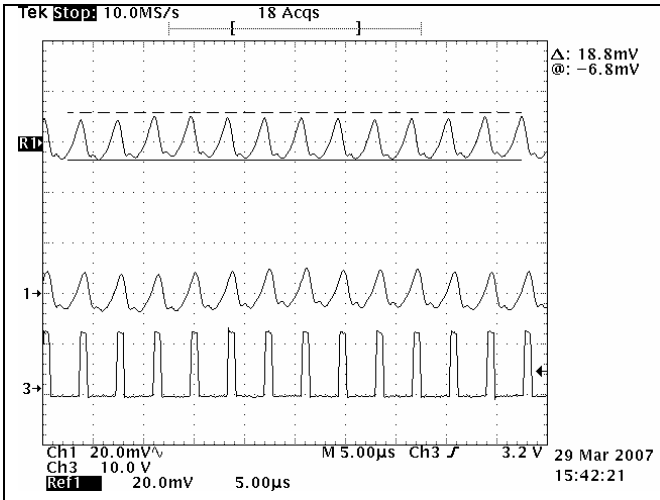
Pdiss: Power dissipation of complete solution
Pdiss L: Power dissipation of output inductor
Pd PB: Power dissipation of PowerBlox IC.

Thermal Performance and Derating

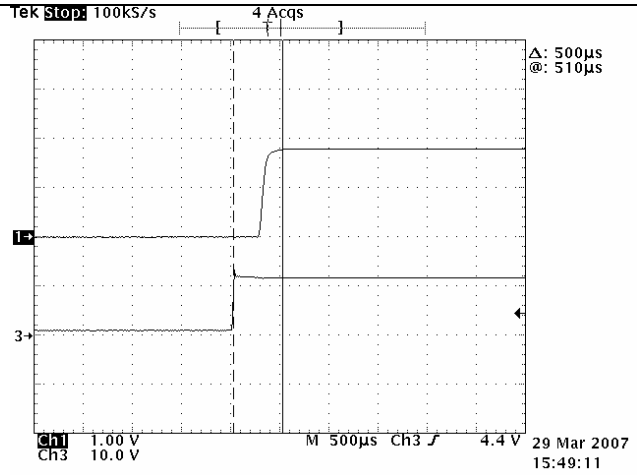
A complete thermal analysis of the PowerBlox IC mounted on various PCB's has been completed and the results are available from our web site. The results show that under the conditions noted above the part would not require any derating even without airflow at full load. The worst case power dissipation at 85°C with no airflow was 2.25 Watts. None of the figures above exceed this, however this data is at room temperature. As temperature increases and efficiency drops the power dissipation will go up. To allow some margin it would be best to recommend 100lfm of airflow when used at 85°C ambient.

For more information see: http://www.sipex.com/files/applicationNotes/ANP25PowerBloxThermalAnalysis.pdf

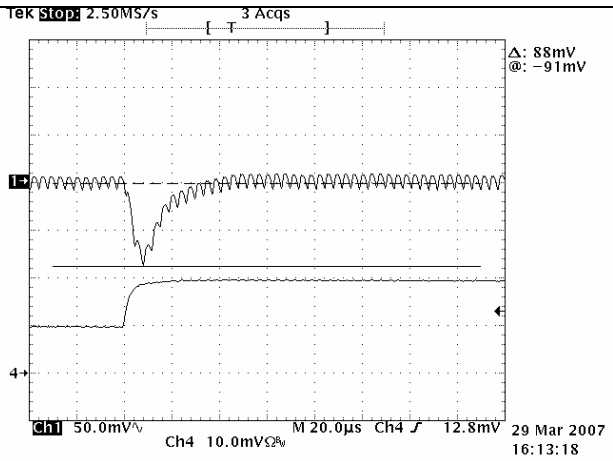
Waveforms



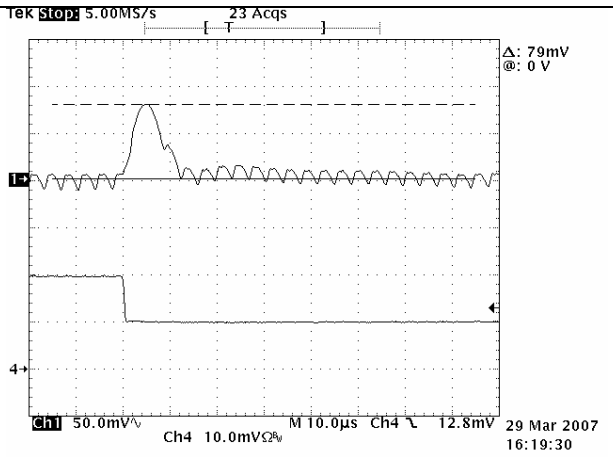
Output Ripple. CH R1: Vout CH1:Vout CH3: LX
R1: Io= 10 Amps CH1: Io= 0 Amps



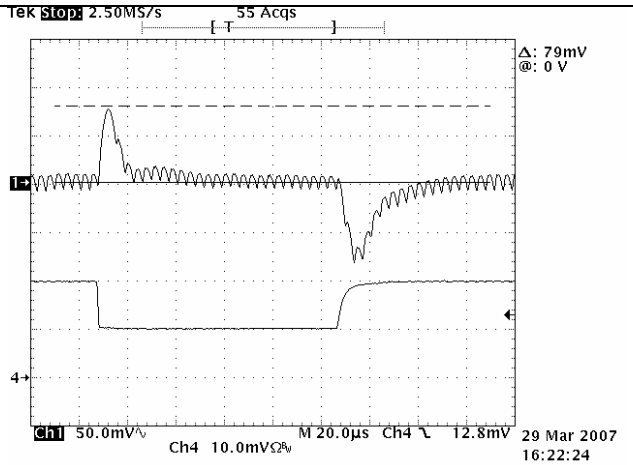
Start-Up Waveform
CH1: Vout CH3: Vin



Transient Response. CH1:Vout CH4:Iout (5A/div)
ΔIo = 1A/uS 50% - 100% Load Step



Transient Response. CH1:Vout CH4:Iout (5A/div)
ΔIo > 1A/uS 100% - 50% Load Step



Transient Response. CH1:Vout CH4:Iout (5A/div)
ΔIo ≥ 1A/uS 50% - 100% - 50% Load Step

Conclusion

By using the Sipex SP7662 and some easy to implement circuits a less expensive alternative to POLA™ parts can be created. The design outlined met or exceeded the required specifications.

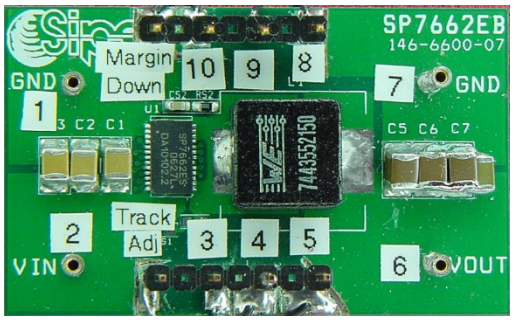


Figure 10 – Complete POLA™ part evaluation board

Appendix

- Full page complete solution with options schematic

Web link to SP7662

http://www.sipex.com/productDetails.aspx?part=SP7662

For further assistance:

Email: Sipexsupport@sipex.com
WWW Support page: http://www.sipex.com/content.aspx?p=support
Sipex Application Notes: http://www.sipex.com/applicationNotes.aspx

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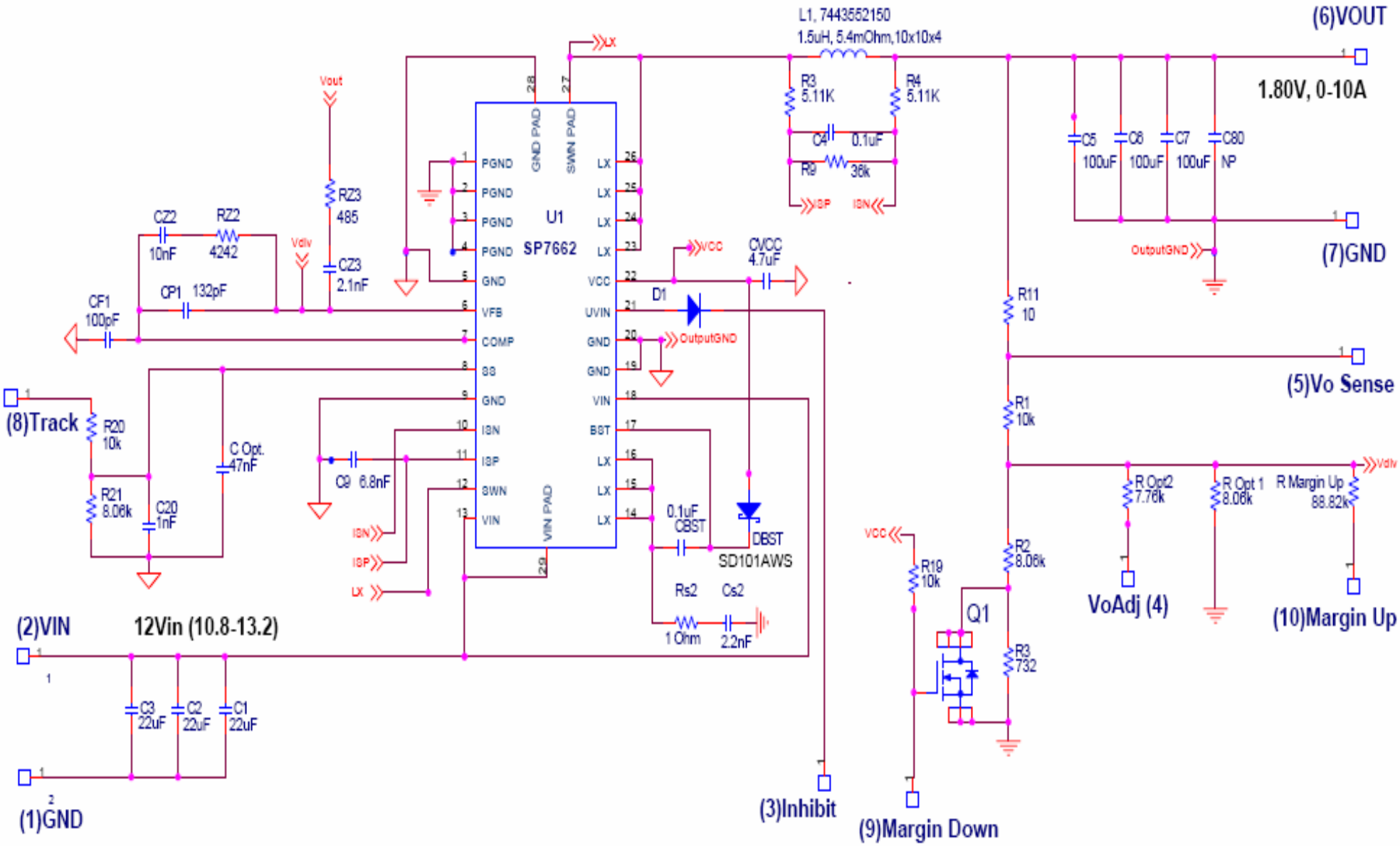

POLA™ Complete Solution Schematic