



Advanced Features of the SP3070E-SP3078E and SP3080E- SP3088E High Performance RS-485 Transceivers

Overview

The SP3070-3078E and SP3080-3088E families of advanced RS-485 transceivers contain a rich feature set designed to simplify the design of robust, high performance RS-485 communication networks. All members of these two new product families remain fully backward compatible to industry standard RS-485 devices, keeping the same footprint and pin locations as earlier products. They are ideal for new designs or as replacements in existing RS-485 or RS-422 systems.

This document describes some of the new features found on SP3070-3078E and SP3080-3088E devices and is intended to help system designers understand how to use these devices most effectively.

General Description

The SP3070E-3078E and SP3080-3088E families include a total of 18 products. SP3070-3078E operate from a 3.3V supply voltage and SP3080-3088E operate from 5V supplies. Each family offers a choice of slow, medium or fast data-rates and either half-duplex, full-duplex or full-duplex with enable/shutdown. Each device contains one differential driver and one differential receiver. All comply with both RS-485 and RS-422 EIA Standards.

Tables 1 and 2 - Product Selection Matrices

3.0 to 3.6V Supply				
Type	Pins	250kbps, Low EMI	500kbps, Reduced EMI	16Mbps, High Speed
Half-duplex	8	SP3072E	SP3075E	SP3078E
Full-duplex, Low Pin-count	8	SP3071E	SP3074E	SP3077E
Full-duplex, Enable/Shutdown	14	SP3070E	SP3073E	SP3076E

4.5 to 5.5V Supply				
Type	Pins	115kbps, Low EMI	500kbps, Reduced EMI	20Mbps, High Speed
Half-duplex	8	SP3082E	SP3085E	SP3088E
Full-duplex, Low Pin-count	8	SP3081E	SP3084E	SP3087E
Full-duplex, Enable/Shutdown	14	SP3080E	SP3083E	SP3086E

Significant Features of the SP3070E-3078E and SP3080E-3088E Families

The SP3070E-3078E and SP3080-3088E families share a number of enhanced features that differentiate these products from other RS-485 transceivers. Below is a list of the “Top Ten” major enhancements that separate these new products from ordinary RS-485 devices.

- 1) 1/8th Unit Load
- 2) Available as half-duplex, full duplex or full-duplex with enable/shutdown pins
- 3) Advanced Failsafe
- 4) Voltage Overload Protection
- 5) Thermal Overload Protection
- 6) Hot Swap and Glitch Protection
- 7) Slew Rate Controlled Driver
- 8) Low Power Shutdown
- 9) Enhanced ESD Protection
- 10) Industry Standard Package Footprints

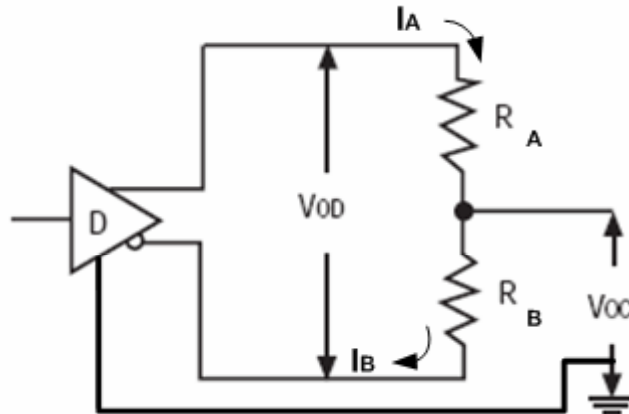
1/8th Unit Load

All devices in the SP3070E-3078E and SP3080E-3088E families are 1/8th Unit Load transceivers. This feature enables large RS-485 networks of up to 256 devices to operate over the full common mode voltage range.

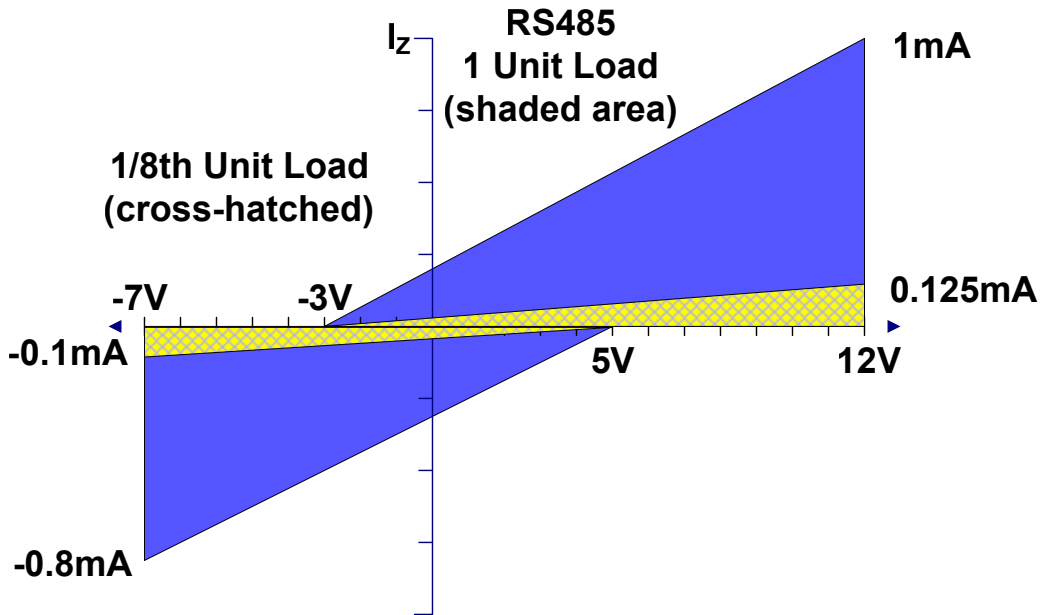
RS-485 is defined to allow multiple transmitters to coexist on a single segment of twisted-pair cable. Only one transmitter may be active and driving at a time but many receivers or transceivers (with driver off) may coexist. Receivers have high input impedance but will absorb some signal-current from the bus. Each additional receiver or transceiver will therefore increase the loading on the drivers. The number of nodes that any segment can support is therefore limited by the strength of the drivers and the load characteristics of each receiver.

A standard RS-485 driver is capable of driving up to 32 "Unit Loads" plus two line-termination resistors of 120Ω each. The EIA-485 standard defines Unit Load in terms of the current load over a common mode voltage range of $-7V$ to $+12V$ from device ground. Common mode voltage is an important factor because at common mode further from device ground the driver must source or sink more current into the load to maintain the same signal margin at a receiver.

The figure below is a simplified electrical model of a driver and load. Each terminal has an input impedance (R_A , R_B) to local ground. Local ground at the load may be offset from the driver's reference ground by some common mode voltage V_{OC} . The driver attempts to maintain a differential voltage V_{OD} across the receiver inputs. Driver current into A and B increases proportionally to the magnitude of V_{OC} .



The dark shaded region in the figure below defines an RS-485 Unit Load. At $+12V$ the current into the load cannot exceed $1mA$. At $-7V$ current cannot exceed $-0.8mA$. A purely resistive load of $12,000\Omega$ fits within this region. The actual load area extends along a $15k\Omega$ slope to points at $-3V$ and $+5V$, allowing for some non-linearity in the actual load.



SP3070E-3078E and SP3080E-3088E devices are 1/8th Unit Load. This means that over the same input voltage range they will load a driver only 1/8th as much. That area is shown in the cross-hatched area of the figure above. At +12V input the current into a 1/8th UL device cannot exceed 125uA.

Typical RS-485 receivers are one Unit Load apiece. An RS-485 driver can maintain signal to 32 unit loads over the -7V to +12V common mode range. With 1/8th Unit Load devices the same driver can support eight times the number of transceivers, up to 256.

Different types of receivers may be mixed in a network. For every 1 Unit Load transceiver you can substitute eight 1/8th UL devices. This may extend the span of existing networks.

RS-422 or V.11 receivers may interoperate with RS-485. However they do not support the full common mode voltage range. Also they may have a lower input impedance of 4kΩ, meaning that each V.11 or RS-422 receiver consumes approximately 3 Unit Loads.

If the common mode voltage is limited, such as by bonding the grounds of all RS-485 nodes, then it may be possible to build very large networks of hundreds of nodes. Using 1/8th UL devices will further increase the number of transceivers.

2. Full-duplex or Half-duplex operation

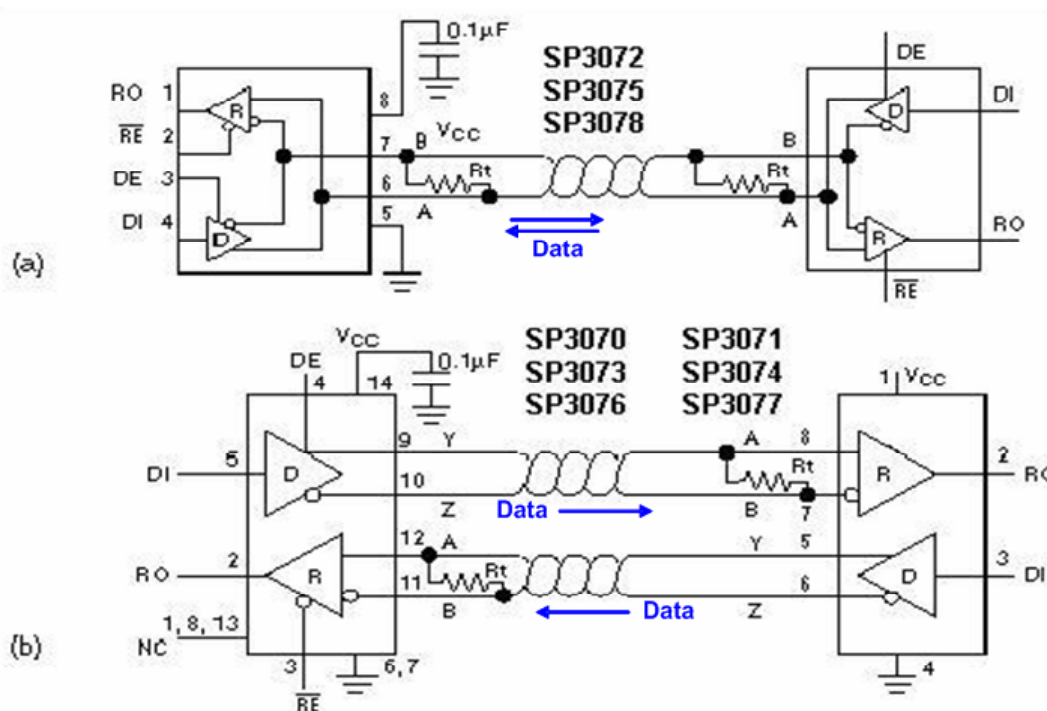
The SP3070E-3078E and SP3080E-3088E families include devices in half-duplex, full duplex and full-duplex with control inputs. All devices are available in industry standard packages and pinouts. This makes Sipex enhanced SP3070 and SP3080 series devices ideal upgrades for existing RS-485 designs.

Half-Duplex is the most commonly used bus scheme for RS-485. Figure 2a shows a typical RS-485 Half Duplex data bus. As few as two or up to 32 Unit Loads, may coexist on the bus. Any node may transmit but only one node may be driving at a time. Data travels bidirectionally on the bus.

The most significant advantage of Half-Duplex is that it requires only a single twisted-pair. This minimizes cable costs. However because only one node at a time is permitted to transmit, half-duplex operation requires bus arbitration to prevent data collisions. The RS-485 standard defines only the electrical characteristics of the interface and does not specify arbitration techniques. Bus arbitration is left up to the end-user. Various proprietary and open-standard interface protocols use RS-485 as a physical media and define methodologies for bus arbitration.¹

Sipex SP3072E, SP3075E, SP3078E, SP3082E, SP3085E and SP3088E are configured for Half-Duplex operation. On these devices the data-bus pins A and B are bi-directional. Driver output enable pin (active high) and receiver enable pin (active low) are opposite polarity and facilitate driver/receiver control on a bidirectional data bus.

Full-Duplex (figure 2b) requires two twisted pairs.



On each wire-pair, data travels only in a single direction. The driver and receiver of each node are physically connected to different wire-pairs. On each pair only a single driver may be active at any given time.

This increases cabling costs but decreases complexity. Full-duplex may be configured point to point (one driver into one receiver) or point to multipoint (one driver and many receivers). In a

¹ : RS485 and RS422 physical topologies are explained in the Application Note ANI13. <http://www.sipex.com/files/ApplicationNotes/RS485%20Topology.pdf>

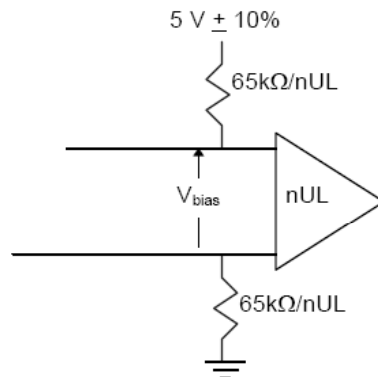
point to point link bus arbitration is not required. In a multipoint full-duplex network one wire-pair may be reserved for the bus master while the other pair is reserved for slaves. This allows both the master and a slave to transmit and receive simultaneously. Therefore overall data throughput in Full-Duplex may be higher than with Half-Duplex.

3. Advanced Failsafe

RS-485 must provide reliable operation in demanding operating environments. If an ordinary differential receiver does not see a differential signal input it is left in an indeterminate state. The advanced failsafe feature on SP3070E-3078E and SP3080E-3088E ensures that the receiver will default to a known output state even if there is no differential signal. This protects the receiver and provides basic fault detection. Advanced failsafe operates if no driver is present, such as during lulls in communication. It also operates in the event of a cable fault, such as if the data cable is accidentally cut, pinched, shorted or unplugged.

A failsafe feature assures a receiver output state will be predetermined if a receiver input becomes tri-state, is left open by fault or cable disconnect, or is shorted together. These three indeterminate states would normally cause the receiver output to be indeterminate.

RS-485 receivers specify that the input threshold be between $\pm 200\text{mV}$ differential. This means that if the differential voltage on a receiver is zero volts, the output state is indeterminate. If the receiver inputs are left floating or unplugged they quickly float to less than 200mV differential unless a failsafe exists. Further, if a receiver's inputs remain close to their detection threshold, any noise may be enough to cause the output to chatter. Chatter will increase power consumption and may drive false signals into the rest of the system.



The standard technique for differential failsafe is to bias the differential lines. Placing a pull-up resistor to a reference voltage on one line and a pull-down to ground on the other line biases the line. The receiver will always see differential voltage even if there is no driver active.

The resistor-bias technique has many drawbacks. A bias reference voltage must be available at all times. If parallel termination is used, it creates a constant DC current path through the bias resistors and the termination, increasing power consumption. Adding bias to the lines reduces the noise margin of valid data signals. It forces the driver to work harder to overcome bias in one direction but makes it easier in the other direction. This introduces skew in the signal which may limit the data rate or otherwise reduce signal integrity.

Designing an optimal resistor-bias network can be surprisingly complex. The engineer must take into account may set up circulating currents, generate EMI and can even damage or overstress some components.

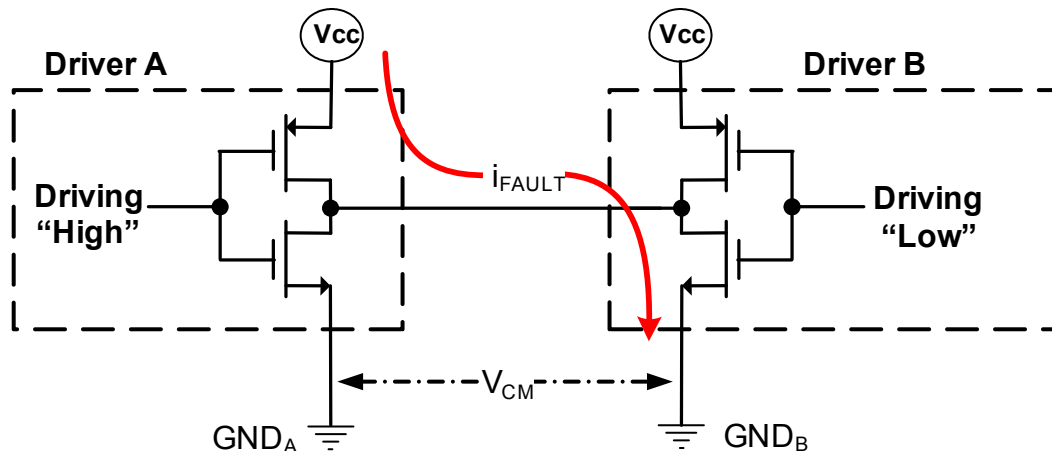
Enhanced transceivers with internal failsafe eliminate the need to add external bias networks to protect the receiver. The internal failsafe circuit on SP3070E-3078E and SP3080E-3088E solve the failsafe problem by setting receiver thresholds between -50mV and -200mV. If a zero volt differential appears across the input stage due to a fault condition, the output is guaranteed to be logic high. The noise margin of 50mV prevents false transitions. This tighter receiver threshold range fits within the RS-485 limits of $\pm 200\text{mV}$ and complies fully with the standard. The receiver must be almost three times more precise and offset to a negative threshold, compared to ordinary RS-485 devices.

4. Driver Voltage Overload Protection

Bus contention is a real danger in RS-485 because multiple drivers may coexist in a shared network. Also RS-485 cabling is often run parallel with other network cables, telephone lines or power wiring. The RS-485 bus may be exposed to accidental short circuits due to cable failures or human error. Lines may pick up excessive voltages through noise coupling. Any of these situations could put excessive voltage into the driver. Driver voltage overload protection in the SP3070E-3078E and SP3080E-3088E prevent drivers from sinking or sourcing excess current if an overvoltage situation occurs.

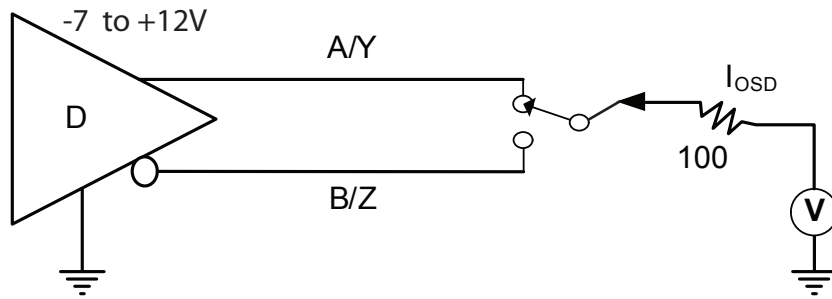
Bus contention is a fault condition and occurs when more than one driver is enabled on a bus at any one time. This is similar to having a short circuit since a driver output represents a low impedance source potential. If one or more drivers are sourcing current while another is sinking current, excessive power dissipation may occur within either the sourcing or sinking driver.

The figure below shows a bus-contention situation. Driver A is attempting to drive the bus high, while driver B is attempting to drive low. Very high fault current can flow from Vcc of driver A, over the bus, into driver B. If a common mode difference in ground potential exists between A and B this exacerbates the problem. Excess current can damage or destroy either or both of the drivers.



Driver short circuit protection limits the output stage drive current if the bus is accidentally shorted to any low impedance potential. This assures ruggedness of the device to prevent permanent failure. The driver current limit provides immediate protection against short circuits over the whole common-mode voltage range. The current limiting activates for driver output current between +/-60mA and +/-250mA. This protection acts continuously and is independent of any other fault protection.

The driver-contention test (shown below) is used to validate the robustness of SP3070E-3078E and SP3080E-3088E devices against contention events. It tests the driver's ability to withstand over-current caused by driver contention. The driver must survive without damage in any logic state while forcing driver outputs to -7V to +12V of common mode.



5. Thermal Shutdown

In the event of a prolonged bus contention or short circuit a built in thermal shutdown protects the device against damage from overheating.

Thermal shutdown is designed to power down the device if the internal transistor junction temperature exceeds a preset target. The trip point for the SP3070E and SP3080E families are set to 165 degrees centigrade. Thermal shutdown is independent of any other fault protection. The thermal-shutdown circuit forces the driver outputs into a high-impedance state. In this way, if the fault is originating on the bus, the SP3070E-3088E will be disconnected from the cause of the fault and continuously protect the device from permanent failure.

6. Hot Swap / Power-Up Glitch Protection

SP3070E-3078E and SP3080E-3088E driver enable (DE) and receiver enable (\overline{RE}) inputs feature glitch protection for hot swap applications. Both the driver and receiver are held inactive for approximately 10 microseconds after initial power-up to allow the system to stabilize before sending or receiving data.

“Hot Swap” refers to situations where power is suddenly applied to all or part of a system. The scenario that gives “hot swap” its name is a when circuit board is inserted into a powered (i.e. “hot”) backplane.

Anytime power is suddenly ramped to a system, differential disturbances to the data bus can cause logic errors. Logic circuits, such as processors, microcontrollers or DSPs often take longer than other system components to power-up and stabilize. During this period, the processor’s logic-output drivers may enter random states or may be held at high impedance and unable to drive the DE and \overline{RE} inputs of these devices to a defined logic level. Leakage currents of only 10 μ A could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance can cause coupling of VCC or GND to the enable inputs. These conditions could improperly enable transceivers without hot swap protection, causing them to send invalid data out onto shared data busses.

For an interface device such as an RS-485 transceiver the consequences of an uncontrolled hot swap situation are particularly severe. If the transceiver is connected to a shared network bus before being powered on, then invalid data may corrupt communications among dozens or even hundreds of nodes. Invalid signals may also cause driver contention.

Hot Swap protection built into the SP3070E-3078E and SP3080E-3088E devices enable glitch-free performance. When Vcc rises, an internal circuit pulls DE low and \overline{RE} high for approximately 10 mi-

croseconds. After the initial power-up sequence, the hot swap circuit becomes transparent, DE and \overline{RE} operate as normal high input-impedance CMOS logic inputs. They can then be driven by standard logic signals.

Fig 6a – DE Hot Swap Test Procedure and Measurement Results

1. Connect a 5100 Ohm pull-up resistor from DE to VCC.
2. Connect a 500Ω resistor from Z to GND (to define Z when the driver is inactive)
3. DI = 0V (makes Z = VCC when active)
4. Switch VCC from 0 to VCC
5. Monitor VCC, DE and Z @ power-up

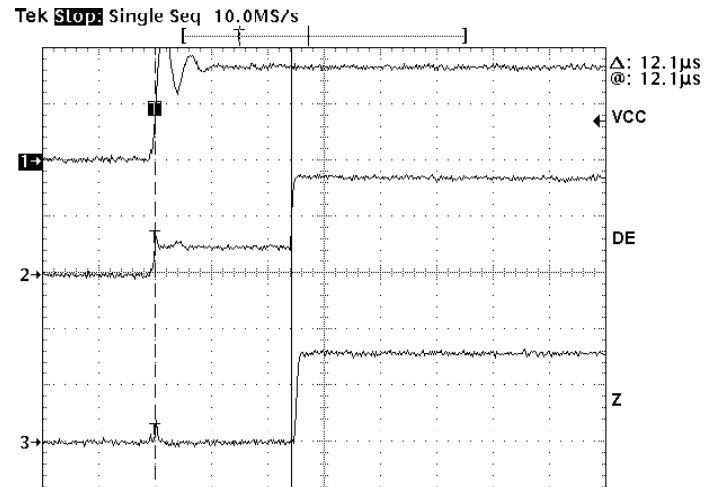
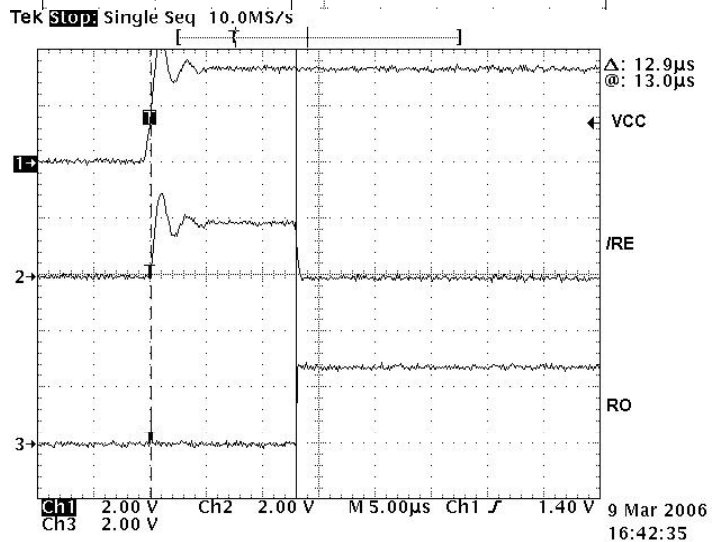


Fig 6b – \overline{RE} Hot Swap Test Procedure and Measurement Results

1. Connect a 5100 Ohm pull-down resistor from \overline{RE} to GND.
2. Connect a 500Ω resistor from RO to GND (to define RO when the receiver is inactive)
3. A = Vcc, B = 0 (makes RO = Vcc when active)
4. Switch Vcc from 0 to Vcc
5. Monitor Vcc, \overline{RE} and RO @ power-up

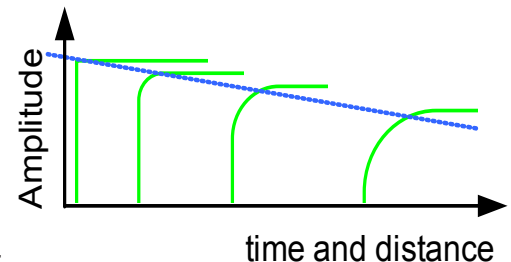


7. Slew Rate Controlled Driver

For maximum data rate choose a high speed transceiver. If EMI is a concern or if operating in severe noise conditions a slew-limited device may be more appropriate. Choosing a slew-limited device can sometimes reduce or eliminate the need for bus termination resistors.

Slew rate control helps to reduce electromagnetic interference (EMI) radiated by a communication network. Slew-rate limiting works by slowing the edges of the RS-485 signal down and therefore reducing the signal's high-frequency components.

As signals travel along a transmission line the higher frequency components attenuate more rapidly than lower frequencies. This causes the signal edges (in the time domain) to become rounded and in extreme cases can diminish the amplitude of the overall signal. This lost energy is radiated out as EMI. Signals with strong high frequencies radiate more than signals made up only of lower frequencies.



The oscilloscope plots in figures 7a and 7b show the effect of slew rate control the transmitted signal. Figure 7a on the left shows a slew limited device, 7b on the right a non-limited device. The top trace (signal 1) is the driver input. The center trace (signal 2) shows the driver output signal. This is the signal on the bus. The bottom trace is a Fast Fourier Transform (FFT) showing the frequency spectrum of the driver output.

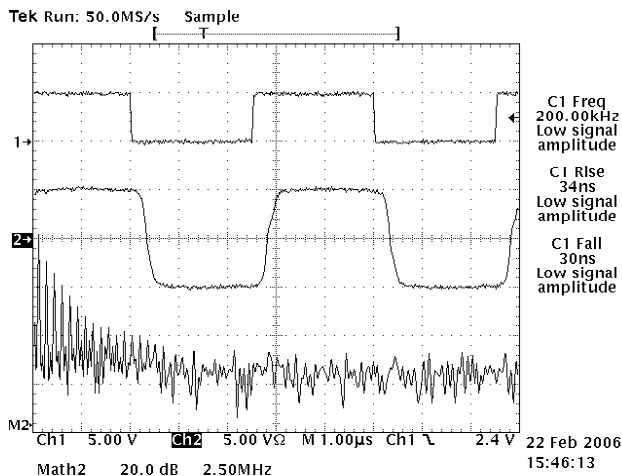


Fig 7a –Driver with slew Limit

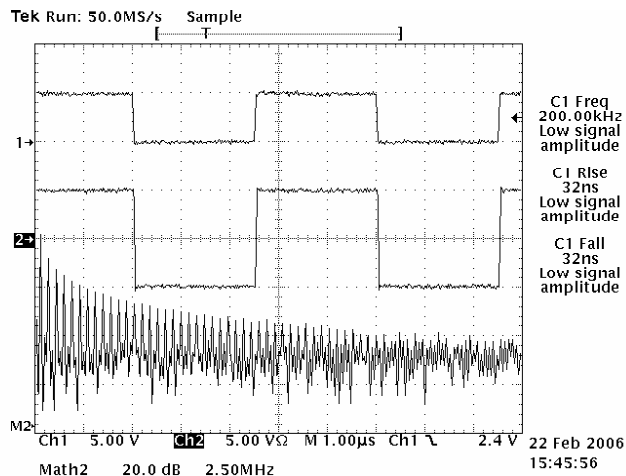


Fig 7b – Driver without Slew Limit

On the driver with slew rate control the driver rise and fall time edges are somewhat rounded. This indicates that high frequency components are being filtered out. The FFT plot shows that signal harmonics are limited to below 5MHz. The driver with no slew rate control has very sharp driver edges and its spectral response shows harmonics well into the 20MHz frequency range.

The SP3070E-3078E and SP3080E-3088E families contain devices with and without slew limited driver outputs. Fully slew rate limited devices have the least high-frequency signal components and therefore the lowest EMI. However this also limits their maximum data rate to 115kbps or 250kbps. High speed devices are not slew limited and can therefore operate at much faster speeds. In the middle are devices that are slew limited to 500kbps that offer improved EMI performance with a high

Table 7c –Maximum Data Rates

Part Number	Type	Maximum Data Rate
SP3080/81/82	Fully Slew Rate Limited	115 kbps
SP3070/71/72	Fully Slew Rate Limited	250 kbps
SP3073/74/75	Slew Rate Limited	500 kbps
SP3083/84/85		
SP3076/77/78	High Speed	16 Mbps
SP3086/87/88	High Speed	20 Mbps

8. Low Power Enable/Shutdown

Sipex RS-485 transceivers are built in low power Analog-CMOS technology. In order to minimize power consumption even further, devices with Driver Enable and Receiver Enable controls enter a 50nA shutdown mode when driver and receiver are disabled.

All half-duplex and the 14-pin full-duplex devices allow independent enable and disable of the driver and receiver. Driver outputs go to a high impedance state when disabled, releasing the bus, allowing other drivers to communicate. DE and \overline{RE} operate at different polarities and can be driven simultaneously using a shared direction-control signal.

Low-power shutdown mode is initiated by bringing \overline{RE} high and DE low. In shutdown, the devices typically draw only 50nA of supply current. The parts are guaranteed not to enter shutdown if \overline{RE} is

high and DE is low for less than 50ns. If both inputs are de-asserted for at least 600ns, the parts are guaranteed to enter shutdown.

Driver Enable times t_{ZH} and t_{ZL} assume the part was not in a low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ assume the parts are awakening from shut down. It takes drivers and receivers longer to become enabled from low-power shutdown mode $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ than from driver/receiver-disable mode (t_{ZH} , t_{ZL})

9. Enhanced ESD Protection

RS-485 interface devices attach directly to signal connectors on the outside of a system enclosure. They may be exposed to ESD events when cables are plugged or unplugged or when a person or object touches the signal pins or connectors. Robust ESD protection is therefore a very important feature.

Most ICs in a typical system are at greatest risk of ESD damage in the factory when the PCB is assembled and the system is being built. After the system is put together they are soldered onto the PCB and shielded within a metal or plastic system enclosure. Interface ICs are designed to attach to an external connector that could be exposed to ESD when a cable is plugged in or when a person or object touches the connector. These interface pins are most likely to see ESD exposure and therefore benefit from additional protection.

Various standardized models are used within the industry to test circuits for Electrostatic Discharge (ESD) susceptibility. These models were developed by different organizations at different times, but each is an attempt to simulate actual situations known to cause ESD problems.

Pins that are exposed to external connector signals (A, B, Y and Z) are designed for ESD protection at the following levels:

- ±15kV Air-Gap Discharge, EN 61000-4-2
- ±15kV Human Body Model
- ±8kV Contact Discharge, EN 61000-4-2

All other signal pins (DI, RO, DE, \overline{RE}) are protected to +/-2kV Human Body Model and +/- 200V Machine Model. All pins are also protected for transient over-voltage and over-current latch-up to JEDEC standard 22.

The Human Body Model (HBM) is based on tests defined in MIL STD 883, method 3015.7. The human model is a 100pF capacitor charged up to the test voltage and discharged into the circuit through a 1.5kΩ resistor. This simulates the effect of static electricity from a person's body discharging through a finger or direct touch.

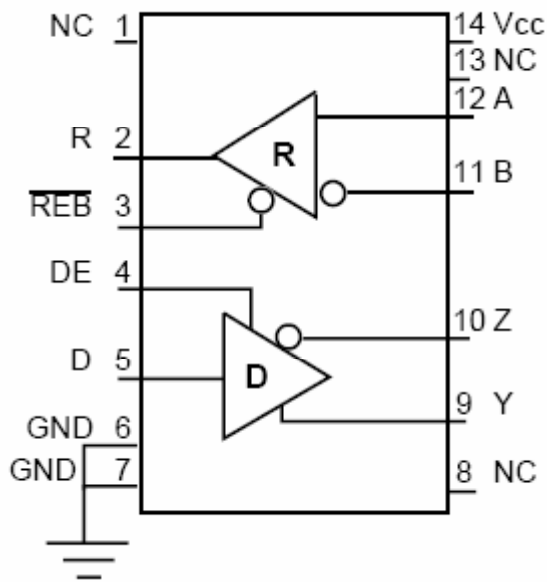
Air-gap and Contact tests are defined in the EN 61000-4-2 (IEC 61000-4-2) standard. The Air-gap test simulates a static discharge from a person holding a pointed metallic object, like a screwdriver, key or tool. As the metal tool gets close to the IC there is a spark discharge jumping a small air gap. In the characterization test a probe of the ESD test-rig is brought close to the IC until a spark happens. Contact discharge puts the test rig in direct contact before discharging with no spark gap. The test rig itself is similar to the one used for HBM but using 150pF and 330Ω. This simulates the faster discharge of the air-gap spark or metal to metal contact as opposed to a human finger-touch. A faster discharge puts more energy into the part more quickly and is more stressful than a slower one.

The machine model uses a direct discharge into the part. It simulates a direct metal to metal contact of a charged device. This type of situation is most likely to occur during manufacturing in a factory with poor static control procedures.

ESD tests are “destructive tests.” The part is tested until it suffers damage. Therefore parts cannot be 100% tested in production, instead a sample of parts are characterized during the product qualification. The test procedure consists of “zapping” pins with a given voltage using the appropriate model and then running the part through electrical tests to detect any performance degradation or loss of functionality.

10. Industry Standard Footprints

The SP3070E-3078E and SP3080E-3088E devices are offered in standard packages and footprints. This enables end-users to easily upgrade existing designs to take advantage of the enhanced performance and functionality these devices provide.

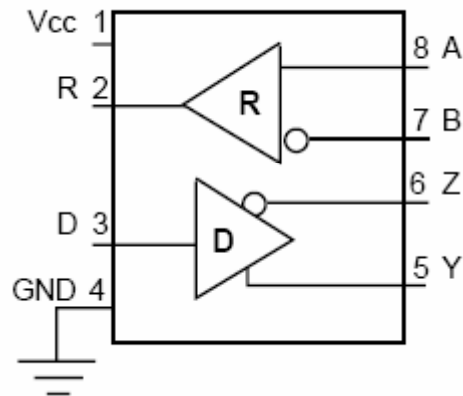


14-Pin Full Duplex, Narrow SOIC:

SP3070E, 250kbps slew limited, 3V
 SP3073E, 500kbps slew limited, 3V
 SP3076E, 16Mbps high speed, 3V
 SP3080E, 115kbps slew limited, 5V
 SP3083E, 500kbps slew limited, 5V
 SP3086E, 20Mbps high speed, 5V

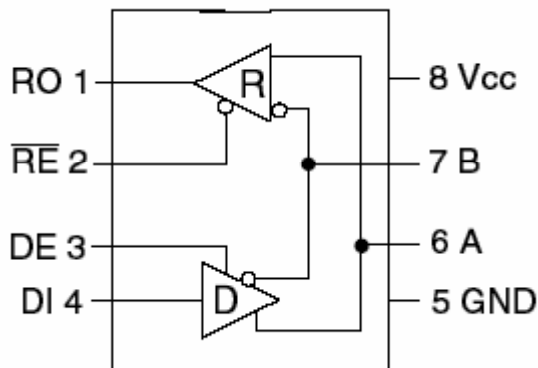
8-Pin Full Duplex, Narrow SOIC:

SP3071E, 250kbps slew limited, 3V
 SP3074E, 500kbps slew limited, 3V
 SP3077E, 16Mbps high speed, 3V
 SP3081E, 115kbps slew limited, 5V
 SP3084E, 500kbps slew limited, 5V
 SP3087E, 20Mbps high speed, 5V



8-Pin Half Duplex, Narrow SOIC:

SP3072E, 250kbps slew limited, 3V
 SP3075E, 500kbps slew limited, 3V
 SP3078E, 16Mbps high speed, 3V
 SP3082E, 250kbps slew limited, 5V
 SP3085E, 500kbps slew limited, 5V
 SP3088E, 20Mbps high speed, 5V



References:

Telecommunications Industry Association TR-30.2/04-12-002, COMMITTEE CONTRIBUTION
Technical Committee TR-30 Meetings, December 10, 2004