The introduction of our SP502 transceiver paved the way for a new generation of multi-mode transceivers that are being designed into next generation networking products. The **SP504** multi-mode transceiver is the latest member of the family and offers: reduced external V.35 termination; V.36 & EIA-530A modes; and receiver tri-state and fail-safe ability.

As with the SP502 and SP503, the **SP504** can be programmed via software to the different available physical protocols and is also drop-in compatible with its predecessors.

The versatility of the **SP504** is ideal for multi-protocol applications such as Frame Relay systems, X.25 routers/switches and multi-protocol routers. These multi-protocol systems will usually contain multiple ports to accommodate the different interfaces. The **SP504** can support all the ports through software and provide convenient DTE or DCE functionality to the port. DTE and DCE configuration is provided on the next page and also in the **SP504** data sheet.

The designer can evaluate the **SP504** with our **SP504 Evaluation Board**. This evaluation board basically allows the user to access the pins directly through probe points on the board. The designer can also access the device by software through the three serial port connectors on the board. Details on the evaluation board can be found in the **SP504** data sheet.
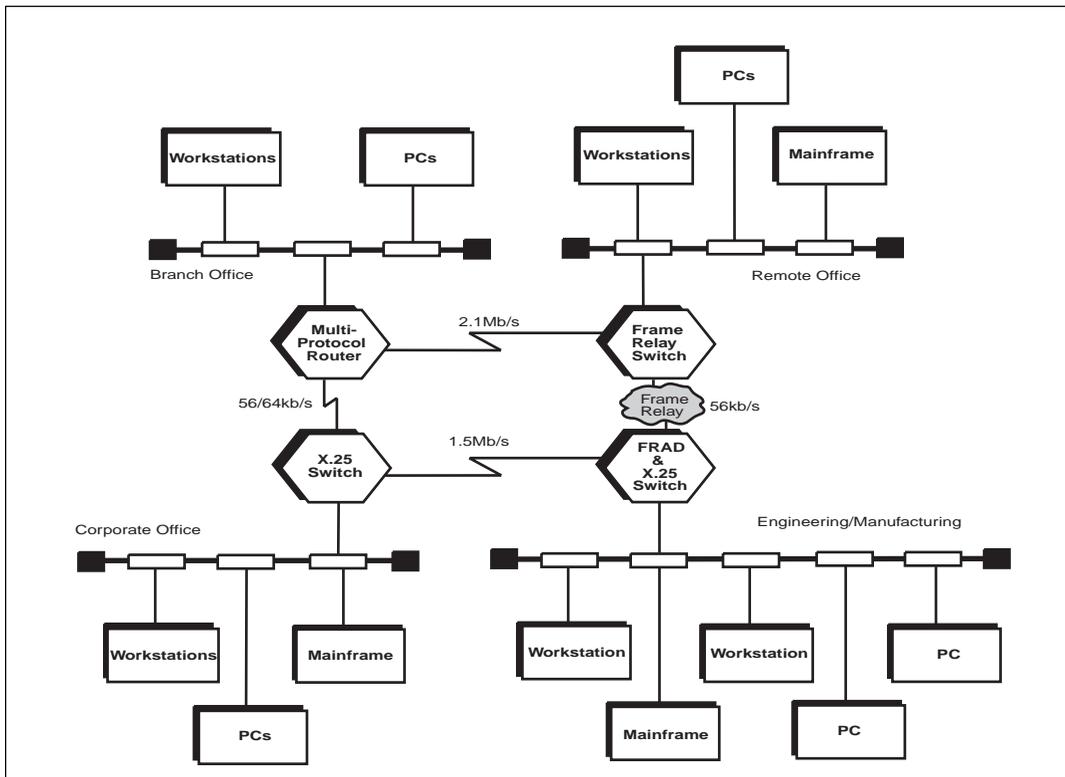
Typical Environment Using Frame Relay and X.25 Systems

# SP504 - Overvoltage and ESD Protection Using Transzorbs
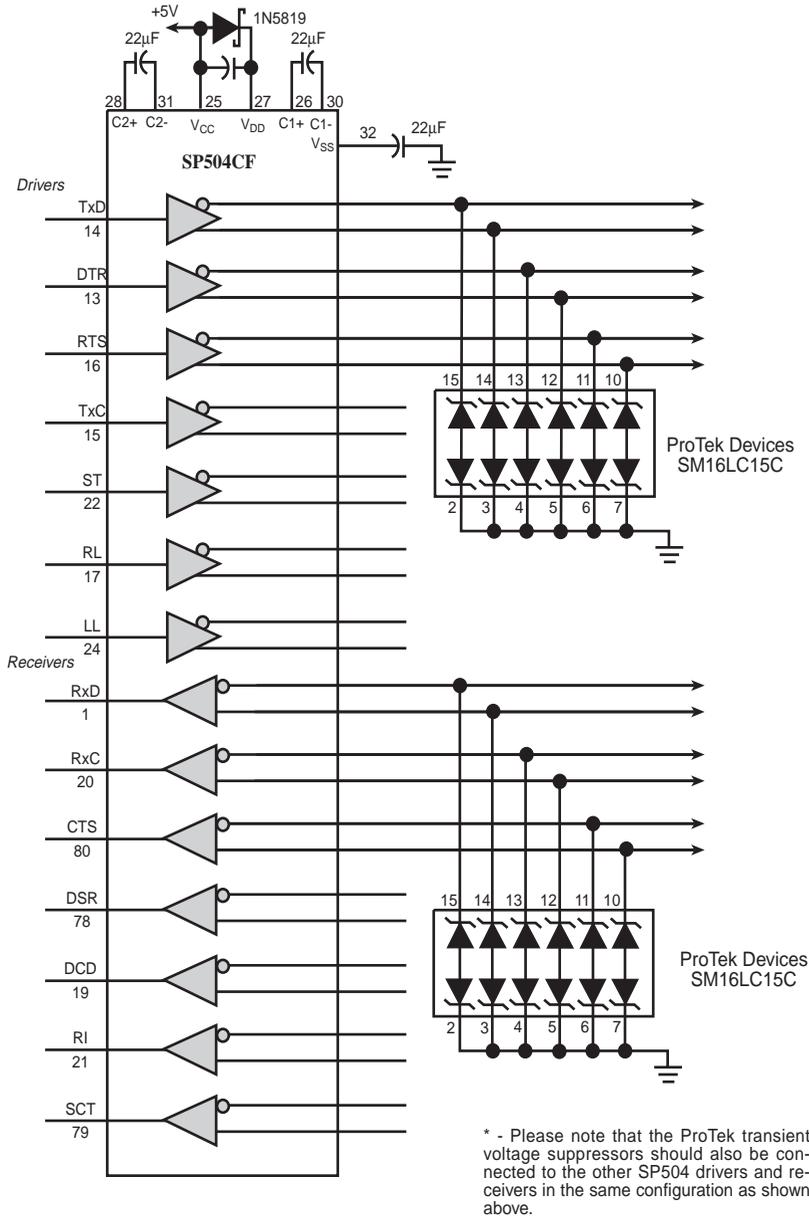
Although the **SP504** is internally protected for ESD and overvoltage, an external transient voltage suppression circuit can be added to increase the level of protection of the device. This may be desired for greater ESD protection or clamping the input or output voltages. The maximum driver output and receiver input voltages should not exceed ±15V.

The **SP504** configuration above uses ProTek Devices'

SM16LC15C TVS devices to protect the receiver inputs and the driver outputs since these pins are directly exposed to the connector and the outside world. The V_{wm} of the TVS can be as low as 5V and high as 15V to cover the RS-232 voltage levels. However, the RS-232 3kΩ to 7kΩ input impedance will not comply if the voltage levels exceed the clamping voltage of the TVS.

ProTek Devices • Tempe, AZ. • 602-431-8101

SP503/504 - One Chip Half-Duplex Configuration
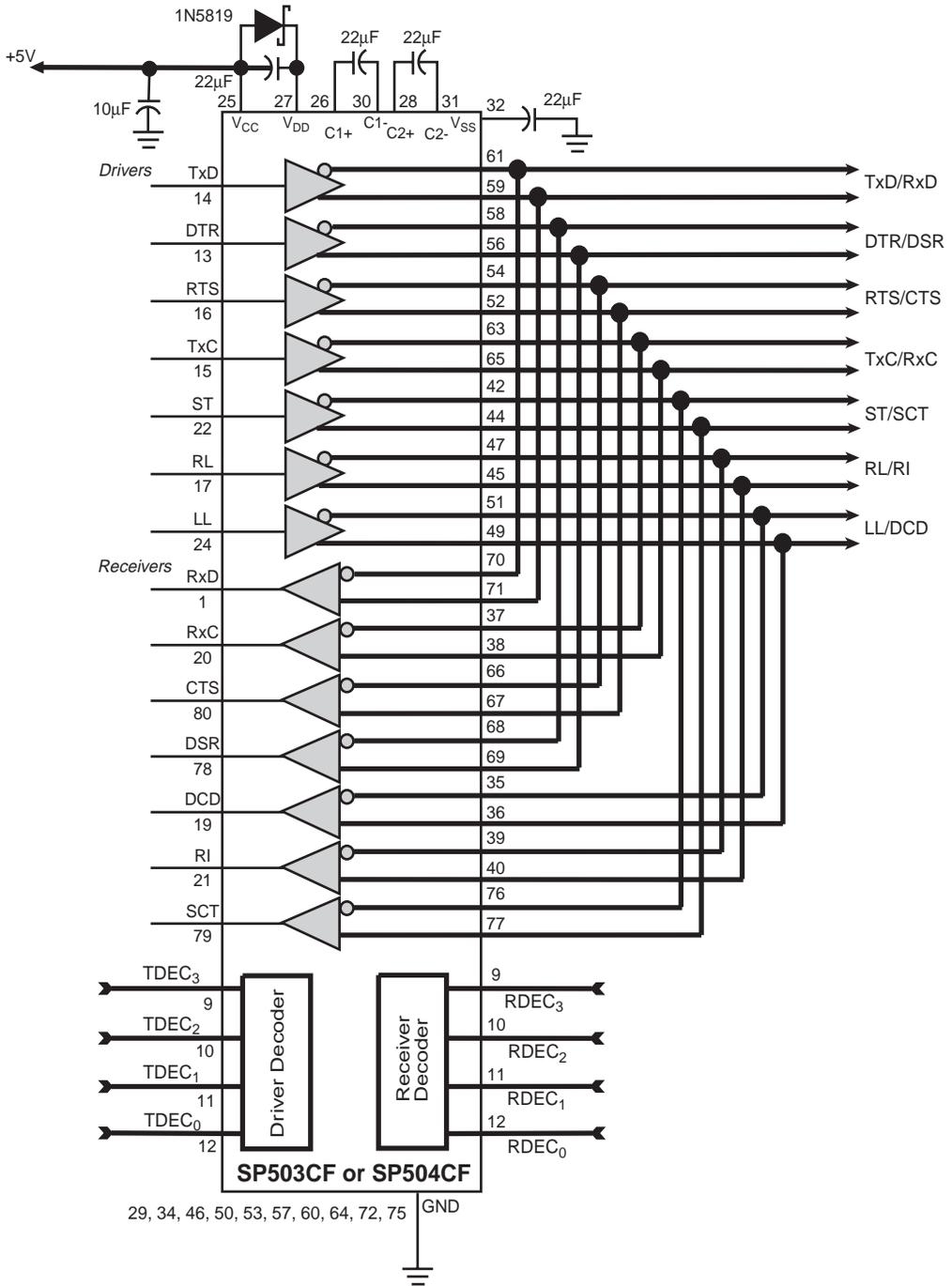
SP504 - DTE/DCE Configuration

Many systems may require the serial port to be configured as either a DTE or DCE. The **SP504** is an ideal candidate for a space saving DTE/DCE solution.

To perform this with the **SP504**, the driver outputs of the first **SP504** are connected back into the receiver inputs of the second **SP504**, and vice versa. The common input/output lines can be routed to the connector and be used as either driver outputs or receiver inputs. Refer to the following page for configuration details.

When the two **SP504** devices are connected as such, one device must be disabled while the other is transmitting and receiving data. Disabling one of the **SP504** devices allows the other to communicate over the serial bus. One is dedicated to a DTE configuration to the serial port and the other is a dedicated DCE device. Disabling the DTE device implies that the serial port will be configured as a DCE, and vice versa.

Disabling the **SP504** drivers are important because a bus contention problem can occur if two drivers are active at the same time. The drivers of the nonactive **SP504** must be tri-stated by writing "0000" into the driver decoder ($TDEC_x$) lines when the I/O lines are used as inputs into the receivers. The receivers do not have to be tri-stated but should be configured so that the receiver input impedance is relatively high ($\geq 12k\Omega$) such as RS-422 or RS-485. The receiver inputs will not affect the signals on the driver outputs if the input impedance is at least $12k\Omega$. If the $RDEC_x$ is configured with "0000", the input impedance defaults to at least $12k\Omega$.

Please note that most of the V.35 termination resistors are internal to the **SP504**. As such, the driver output impedance during tri-state is approximately $20k\Omega$. This should not affect or degrade the incoming driver signal from the other end. Refer to the waveform graphs in the next few pages. The "DTE" waveforms capture the driver and receiver signals at the serial port containing the two **SP504** devices. The "DCE" waveforms are measured in the **SP504** at the other end. For example, the TxD driver output on the DCE side corresponds to the RxD receiver on the DTE side (side containing two **SP504** devices). Similarly, the TxC driver output on the DTE side should be the same as the RxC receiver input on the DCE side.
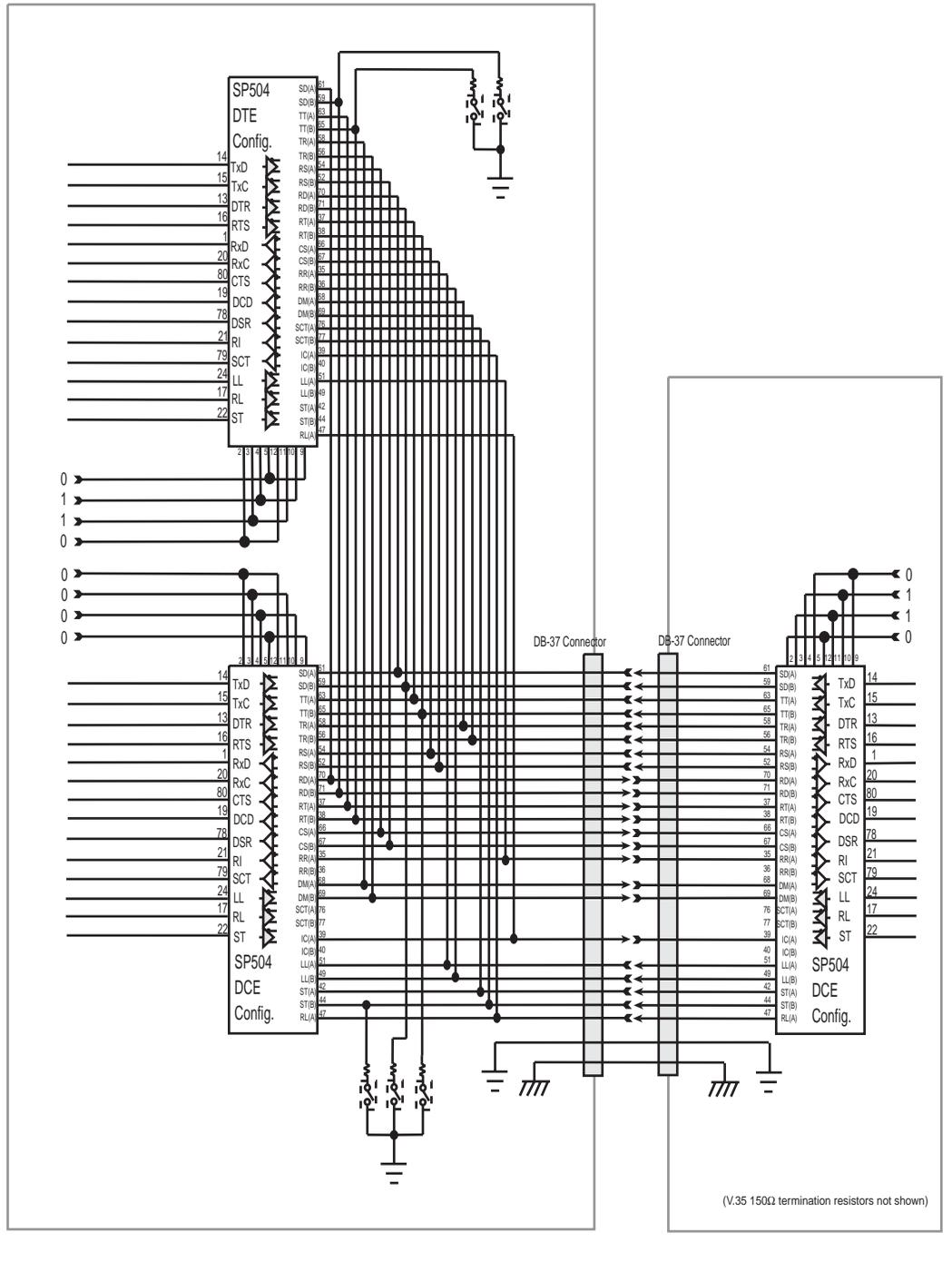
Even though the signal is not degraded, the lower impedance basically adds the driver output impedance ($20k\Omega$) and the receiver input impedance in parallel. When the active **SP504** is configured to RS-232 mode, the typical receiver input impedance is $5k\Omega$ which will yield $4k\Omega$. When in the other modes except V.35, the typical input impedance is $15k\Omega$ which yields $7.5k\Omega$ when the receivers are configured in differential mode (i.e. RS-422, RS-449, V.36, etc.) which is still greater than the $4k\Omega$ minimum requirement for RS-422 and RS-423. The input impedance for the V.35 receiver is typically 100Ω. The driver tri-state impedance will decrease the input approximately 0.5Ω to 1Ω given that the external 150Ω termination resistor is switched off or disconnected from the non-inverting driver output of the disabled **SP504**.
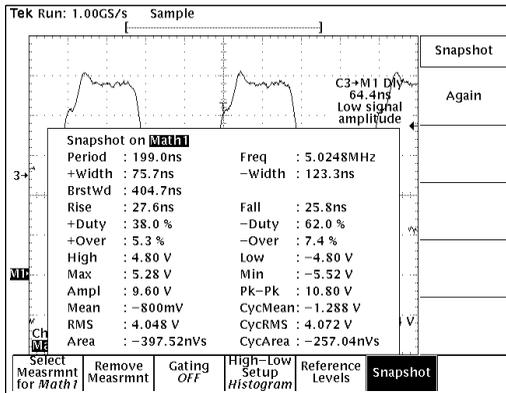
This configuration will allow the proper data communications between DTE and DCE. However for NET1/NET2 certification testing, the driver outputs must be physically disconnected from the receiver inputs. The common I/O paths will interfere with various impedance and current testing for the driver or receiver in V.28, V.11 and V.35 modes.

The tri-state enable and disable timing must be considered. Given two systems, each configured in DTE/DCE operation, containing two **SP504's** each, System 1 is the DTE, and System 2 is the DCE. Assume System 1 is now configured to a DCE and System 2 is configured to a DTE; the two **SP504** devices within each system will have to switch states. If System 1 switches to DCE before System 2 tri-states its driver, the bus will share driver outputs until System 2 switches to DTE, thus causing bus contention problems. In both systems, the active **SP504** should be tri-stated first before enabling the tri-stated **SP504**. Although the bus contention will not damage the **SP504** devices, it should be avoided to prevent short circuit currents at the driver outputs.
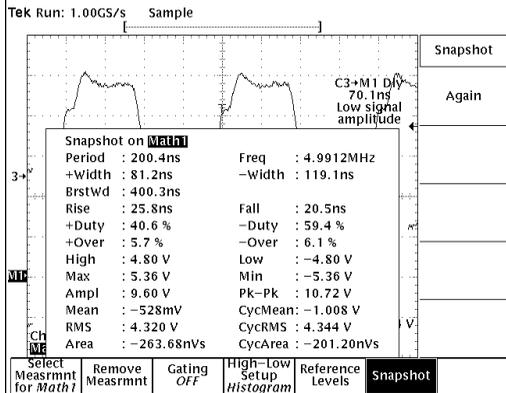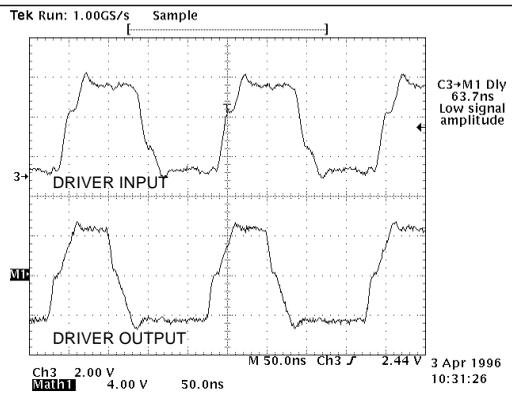
One last consideration for DTE/DCE hookup is the charge pump capacitors. Many have inquired about sharing the 22μF caps. For a minimal requirement, the C1 and C2 capacitors must be separate for each **SP504** device. Although this can be functionally done, Sipex does not recommend this practice. Please be aware that if one **SP504** becomes nonfunctional, it can affect the other **SP504** as well.

DTE/DCE Serial Port Configuration with the SP504

(V.35 150Ω termination resistors not shown)

Waveform for TxD Input → Output; DCE, RS-422 mode @ 10Mbps

Waveform for TxD Input → Output; DTE, RS-422 mode @ 10Mbps
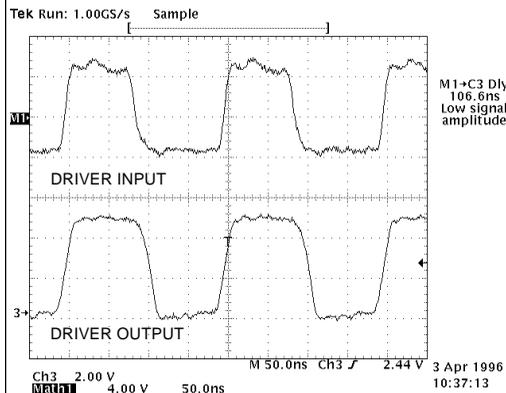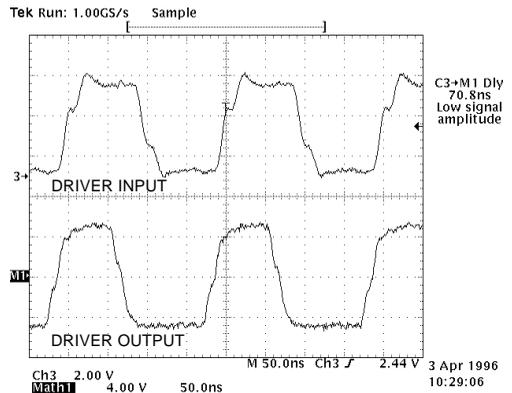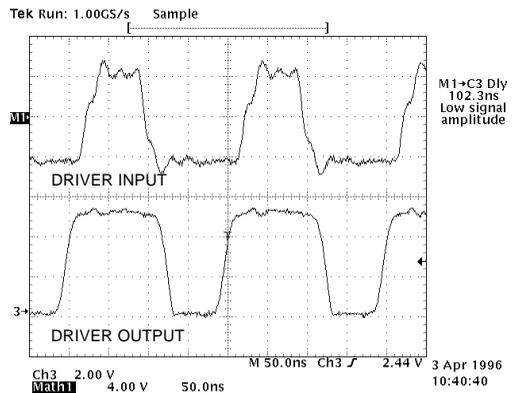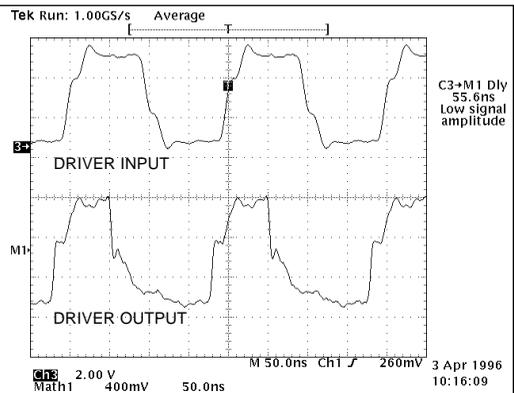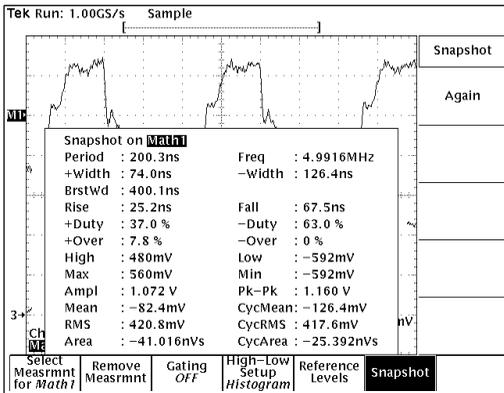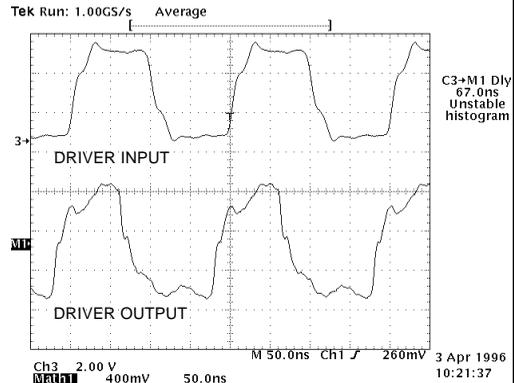

Waveform for RxD Input → Output; DCE, RS-422 mode @ 10Mbps

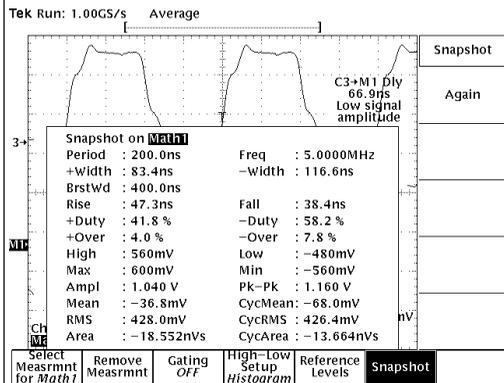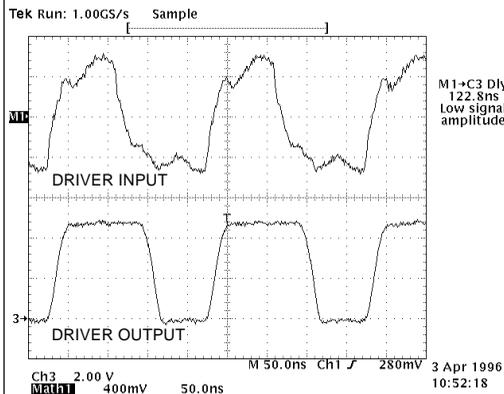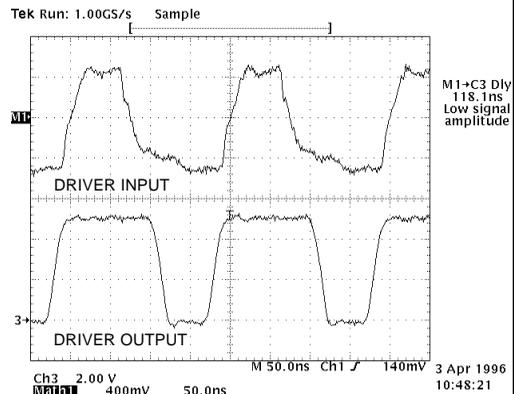Waveform for RxD Input → Output; DTE, RS-422 mode @ 10Mbps

Tek Run: 1.00GS/s   Sample

Snapshot

Again

Snapshot on Math1
Period	: 200.3ns	Freq	: 4.9916MHz
+Width	: 74.0ns	−Width	: 126.4ns
BrstWd	: 400.1ns		
Rise	: 25.2ns	Fall	: 67.5ns
+Duty	: 37.0 %	−Duty	: 63.0 %
+Over	: 7.8 %	−Over	: 0 %
High	: 480mV	Low	: −592mV
Max	: 560mV	Min	: −592mV
Ampl	: 1.072 V	Pk−Pk	: 1.160 V
Mean	: −82.4mV	CycMean: −126.4mV	
RMS	: 420.8mV	CycRMS	: 417.6mV
Area	: −41.016nVs	CycArea: −25.392nVs	

Select Measrmnt for *Math1* | Remove Measrmnt | Gating *OFF* | High−Low Setup *Histogram* | Reference Levels | Snapshot

Tek Run: 1.00GS/s   Average

C3→M1 Dly 55.6ns Low signal amplitude

DRIVER INPUT

DRIVER OUTPUT

M1▸

Ch3 2.00 V   M 50.0ns Ch1 ∫   260mV   3 Apr 1996
Math1   400mV   50.0ns   10:16:09

Waveform for TxD Input → Output; DCE, V.35 mode @ 10Mbps

Tek Run: 1.00GS/s   Average

Snapshot

Again

C3→M1 Dly 66.9ns Low signal amplitude

Snapshot on Math1
Period	: 200.0ns	Freq	: 5.0000MHz
+Width	: 83.4ns	−Width	: 116.6ns
BrstWd	: 400.0ns		
Rise	: 47.3ns	Fall	: 38.4ns
+Duty	: 41.8 %	−Duty	: 58.2 %
+Over	: 4.0 %	−Over	: 7.8 %
High	: 560mV	Low	: −480mV
Max	: 600mV	Min	: −560mV
Ampl	: 1.040 V	Pk−Pk	: 1.160 V
Mean	: −36.8mV	CycMean: −68.0mV	
RMS	: 428.0mV	CycRMS	: 426.4mV
Area	: −18.552nVs	CycArea: −13.664nVs	

Select Measrmnt for *Math1* | Remove Measrmnt | Gating *OFF* | High−Low Setup *Histogram* | Reference Levels | Snapshot

Tek Run: 1.00GS/s   Average

C3→M1 Dly 67.0ns Unstable histogram

DRIVER INPUT

DRIVER OUTPUT

Ch3 2.00 V   M 50.0ns Ch1 ∫   260mV   3 Apr 1996
Math1   400mV   50.0ns   10:21:37

Waveform for TxD Input → Output; DTE, V.35 mode @ 10Mbps

Tek Run: 1.00GS/s   Sample

M1→C3 Dly 122.8ns Low signal amplitude

DRIVER INPUT

DRIVER OUTPUT

Ch3 2.00 V   M 50.0ns Ch1 ∫   280mV   3 Apr 1996
Math1   400mV   50.0ns   10:52:18

Waveform for RxD Input → Output; DCE, V.35 mode @ 10Mbps

Tek Run: 1.00GS/s   Sample

M1→C3 Dly 118.1ns Low signal amplitude

DRIVER INPUT

DRIVER OUTPUT

Ch3 2.00 V   M 50.0ns Ch1 ∫   140mV   3 Apr 1996
Math1   400mV   50.0ns   10:48:21

Waveform for RxD Input → Output; DTE, V.35 mode @ 10Mbps

SP504 - Switching the 150Ω V.35 Termination Resistor

The **SP504** requires one 150Ω resistor to ground on each non-inverting (b) driver output. The 150Ω resistor to ground is necessary to comply with the V.35 short circuit impedance of 150Ω±15Ω. The resistors will need to be switched out when V.35 mode is not active. To perform this, the designer can use one of two methods: add a relay or switch in series with the resistor or implant the resistors inside the V.35 cable.

Adding the resistors to the cable is relatively easy. In DTE mode, two drivers are usually active, therefore you will only need two resistors. The 150Ω resistors can be connected individually from pin S (data) to signal ground (pin B) and pin W (clock) to signal ground (pin B) of the V.35 ISO-2593 connector.

For DCE applications, an additional driver may be used for a secondary clock signal. If a cable is used on the DCE end, a conversion or "mini" cable is necessary to insert the resistors and route the proper signals to the DTE cable. The resistors can be connected from pin S (data), pin W (clock) and an unassigned pin (2nd clock) to signal ground, pin B. Of course the pins on the

"mini" cable will have to be routed to the appropriate end on the DTE V.35 cable. (ie. pin S, pin W and the unassigned pin will be routed to pin T, pin X and pin AA, respectively, on the DTE end.)

Another method is to include the 150Ω resistors on the printed circuit board with the **SP504** adding switches or relays. This method may be preferred if a common connector/cable (ie. DB-25) is used for V.35 and some other mode. The switches must have low on-resistance, preferably less than 1Ω. NMOS FETs can be used as configured on the opposite page. The gate of the NMOS device is connected to pin 18 of the **SP504**. This pin is HIGH when the **SP504** is in V.35 mode and goes LOW in all other modes. Pin 18 is not described in the data sheet for the **SP504** but can be used to control the switching of the FETs or relays.

Sipex recommends Siliconix's LITTLE FOOT™ MOSFET devices such as the Si9959DY™ Dual N-Channel Enhancement-Mode MOSFET. The $r_{DS(on)}$ is typically less than 0.3Ω and the devices are in 8-pin SOIC packages.
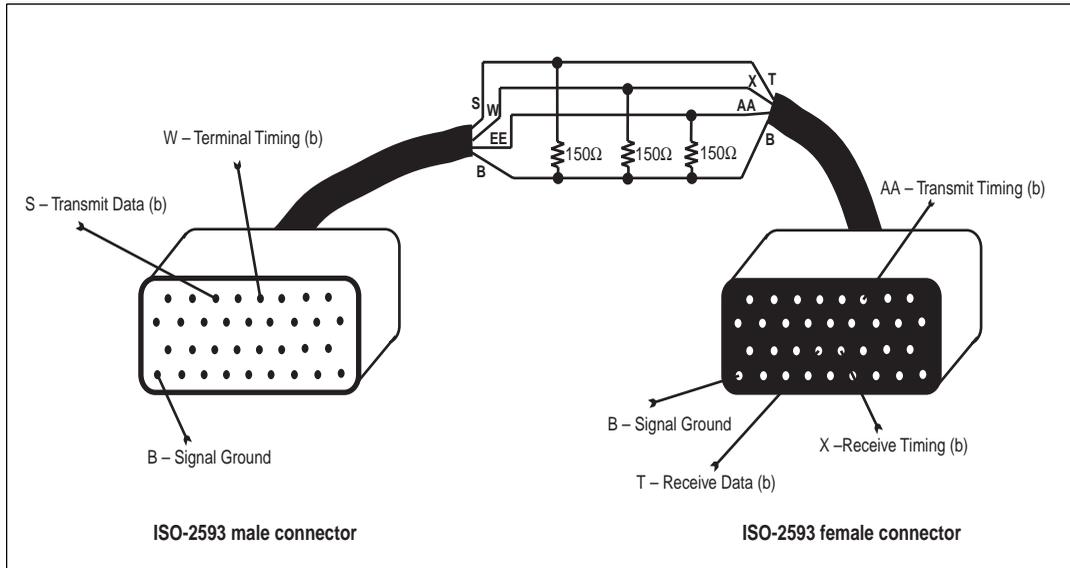
Termination Resistor Implementation in the Cable

™ - LITTLE FOOT is a trademark of Siliconix, member of TEMIC Group.
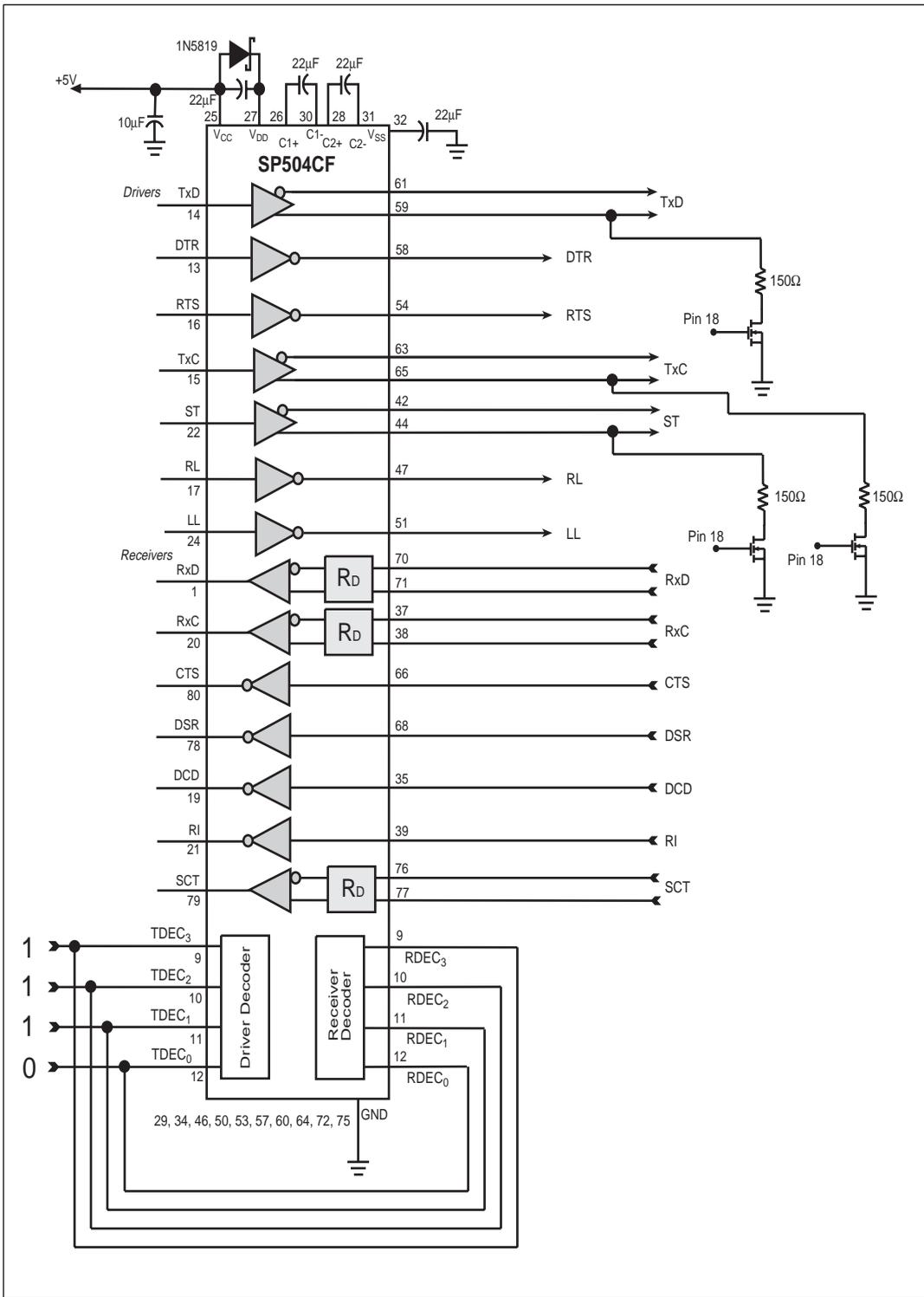
Termination Resistor Implementation on PC Board.

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP504CF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) QFP

Sipex
Corporation

SIGNAL PROCESSING EXCELLENCE