APPLICATION NOTE ANI3

Using Sipex SP3508 Multi-Protocol with QUICC™ or PowerQUICC™ Communications Processors

A Sipex SP3508, SP508 or SP509 can provide a flexible serial port physical interface for a QUICC™ or PowerQUICC™ communications processor. The QUICC can support HDLC, SDLC, LAP-B, BISYNCH or UART data framing and either synchronous or asynchronous operation.

Sipex SP3508 and related devices are single-chip multi-transceivers that are configurable into many types of serial ports. Standardized port configurations include EIA-530/530A, V.35, RS-323, RS-422, X.21, V.24, RS-449 and V.36. Others protocols such as Appletalk™, PROFIBUS™ and many other proprietary port types are also possible.

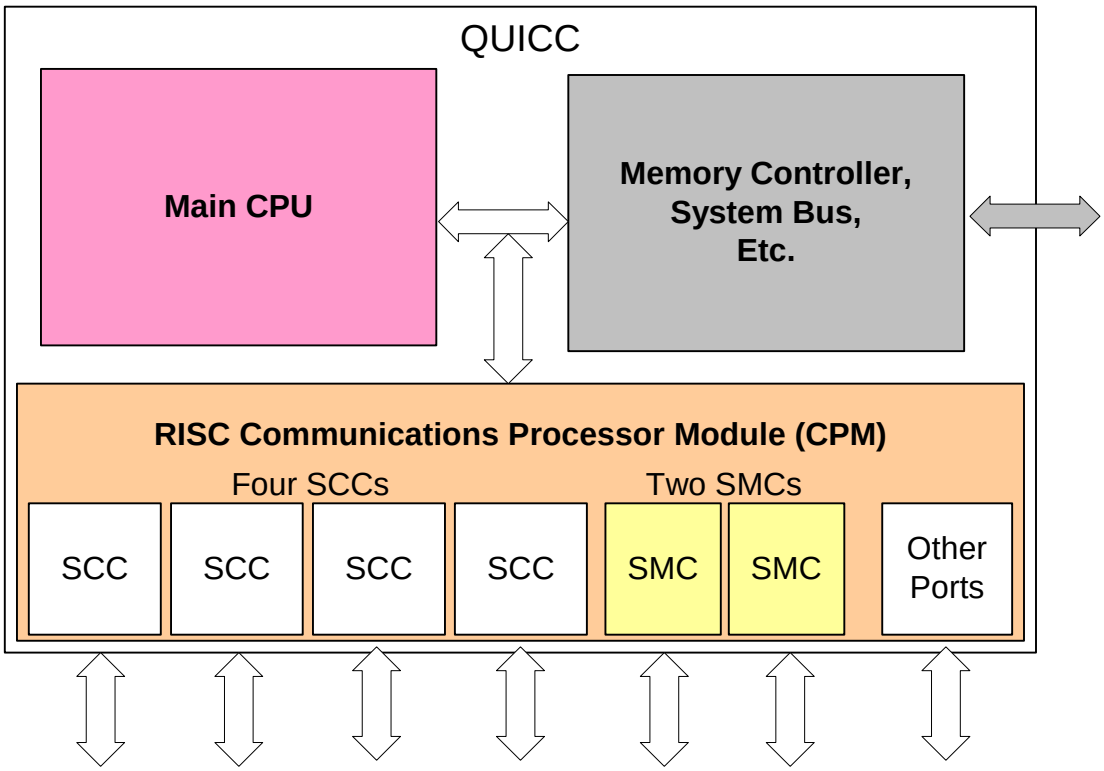
Typical applications would include:

- routing, bridges or gateways between different networks
- data or voice aggregation and dis-aggregation (Nx64, Nx56, fractional T-carrier)
- network security, management, grooming or diagnostics
- interconnect to wide area and public network access (CSU/DSU, FRAD, ISDN)
- communications on RS-485, RS-232, ARCNet, MIL-STD-188, PROFIBUS, etc.
- mainframe or server connections
- connectivity to PBX, video-conferencing systems and high speed modems
- voice and data encryption and security
- wireless, microwave or satellite base stations

QUICC™ Architecture and SCCs

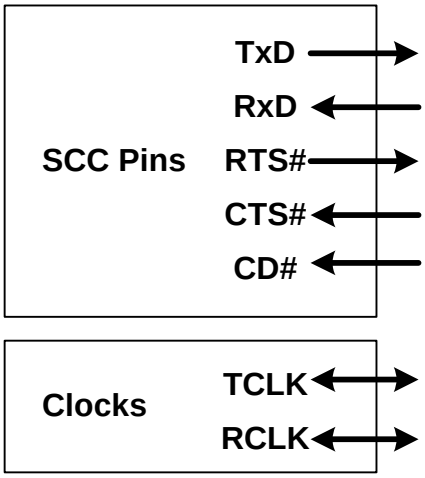
The original QUICC™ (QUad Integrated Communication Controller) devices from Motorola are based on the 68000 microprocessor core. The PowerQUICC™, PowerQUICC II, III and similar devices are based on PowerPC. All devices of this family share a similar architecture for their Serial Communications Controller (SCC) interface. As the name suggests, most QUICC™ family devices have four SCCs. Multiple QUICC processors can be linked together to increase the number of SCC channels. In addition there are two Serial Management Controllers (SMC), which are reduced-function serial ports used for console or diagnostic access. Most QUICC devices have two to four general purpose parallel interface ports that can be used as general purpose input or output signals.

QUICC™ Architecture - Simplified Block Diagram



Each SCC is an independent flexible serial controller that can be programmed for a variety of interfaces, synchronous or asynchronous; everything from RS-232 to Ethernet to ATM. The SCC does not include physical interface for serial communication, only the logic. External line drivers, receivers or transceivers are required for the physical interface. Sipex multiprotocol transceivers such as SP3508, SP508 and SP509 are easily configurable for many different protocols using only a single SCC and a single multiprotocol transceiver IC.

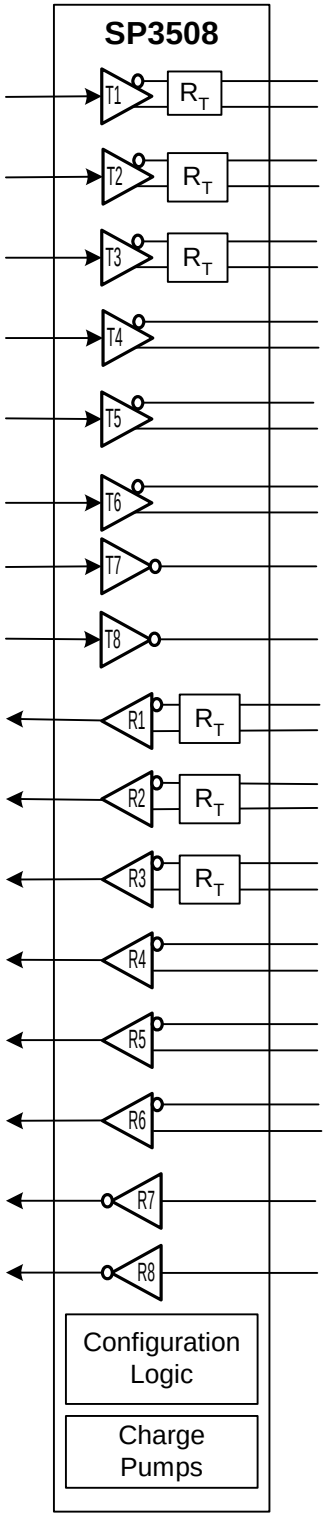
Each SCC has direct control over seven external pins. The Non Multiplexed Serial Interface (NMSI) pins include two data pins (TxD data output, RxD data input), two clock pins TCLK and RCLK, and three modem-control pins RTS# output, CTS# input and CD# input. Additional signals may be supported using general purpose inputs and outputs.



The signal names and directions reflect their function in a DTE configuration, but an SCC may be programmed to operate as either DTE or DCE.

For synchronous protocols each SCC can select clock signals independently for send and receive. Timing can be derived directly from signals on external pins, from onboard baud rate generators or synchronized from onboard digital PLL. Once clock sources are selected they are given internal names of Transmit Clock (TCLK) and Receive Clock (CLK). If several channels are running at the same clock rate they may share the same clock signal.

Simplified Block diagram of SP3508

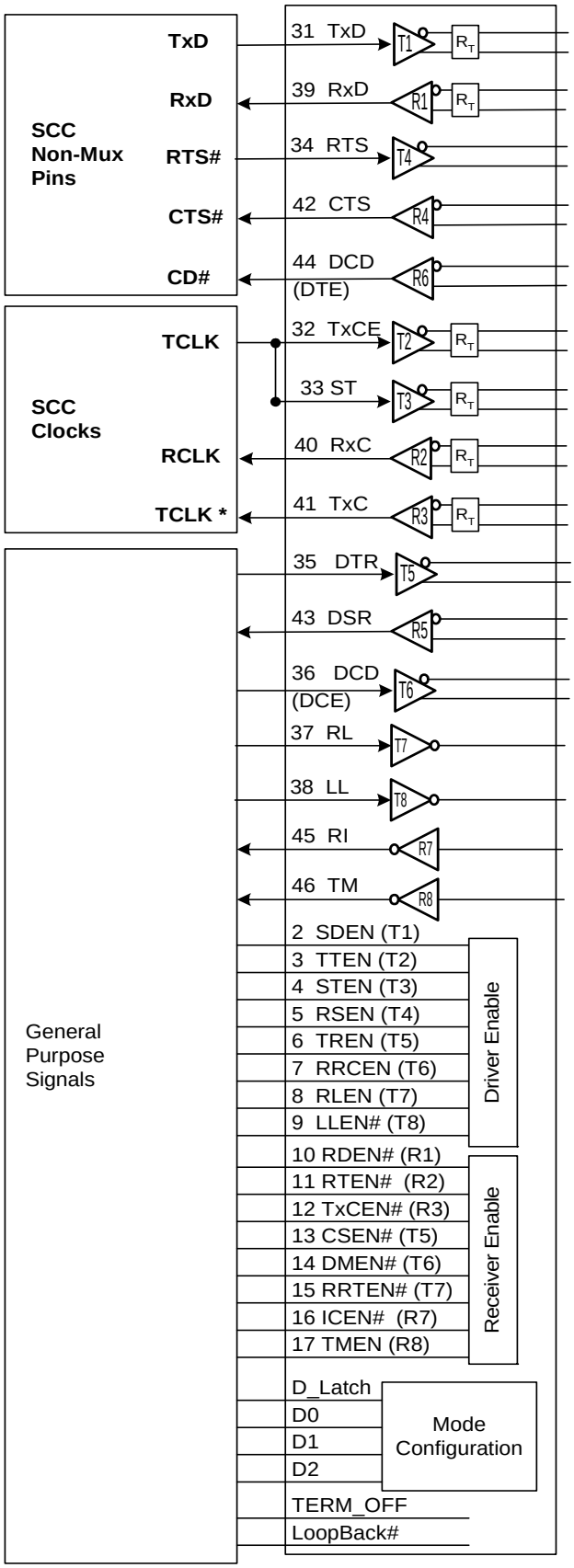


The SP3508, SP508 and SP509 are all highly integrated multiprotocol serial transceivers. Each have a total of 8 drivers and 8 receivers and can be configured to support a variety of standard serial port standards.

SP3508, SP508, SP509 Feature Overview:

- Single power supply. The SP3508 is a 3V device. SP508 and SP509 operate at 5V.
- All signaling and termination voltages are generated from the onboard charge pumps. Charge pumps require only external capacitors (no inductors)
- Total of 8 drivers and 8 receivers
- High data rates. SP3508 and SP508 are capable of 20Mbps for differential NRZ or NRZI signals. SP509 can run as fast as 40Mbps.
- Independent tri-state/enable pins for each driver and receiver
- Three drivers and three receivers can be configured for either V.11, V.28 or V.35 (app II) electrical parameters. These channels are ideal for high speed clock and data signals. The three receivers feature built in cable termination for V.11 and V.35, which eliminates the need for external termination networks. The three drivers have built in termination networks for V.35 mode.
- An additional three drivers and three receivers can be configured for V.11 or V.28 and are ideal for modem control signals.
- Three drivers are configurable for V.10, which is used for Category II signals in EIA-530, EIA-530A, RS-449 and for some signals in AppleTalk.
- Two drivers and two receivers are single-ended only and can be used for test-mode, loopback or optional signals.
- Pre-configured modes for EIA-530, EIA-530A, V.35, V.36, RS-449, X.21 and RS-232
- Robust 15kV ESD protection on driver outputs and receiver inputs
- Internal loop-back mode for device diagnostics
- Latched configuration input pins
- Termination disable pin for multi-drop bus or test equipment
- Low power shutdown mode with all drivers and receivers at high impedance
- Designed for NET1/NET2 and TBR-2 compliance

Connection Example between SCC and SP3508



* Depending on protocol and configuration, clock signals may be sourced from either DTE or DCE both for transmit timing and receive timing. Refer to discussion on co-directional and contra-directional timing.

Unused drivers or receivers can be inactivated using enable pin. Or, enable signals may be ganged together to enable/disable all. Note that LLEN# (T8) and TMEN (R8) have opposite polarity from other driver and receiver enables

When D_Latch = 1, configuration pins D0-2 are latched so they may be muxed with other signals.

TERM_OFF has internal pull-down
LoopBack# has internal pull-up

Signal Descriptions

The hookup diagram above shows an example connection between an SCC and the SP3508. The SP3508 enables a single SCC to be configurable for many serial protocols.

The non-multiplexed pins and clock pins on the SCC implement the high-priority signals used in most serial protocols. Other signals may be connected using general purpose inputs and outputs. Many of these slower signals may be multiplexed onto shared pins, permanently tied high or low, may be controlled by latches or even by manual switches, depending on the implementation.

Data In and Out (TxD, RxD)

Separate data send and receive lines allow for simultaneous communication in both directions (full duplex).

Data payload and clocks are the highest priority signals in a serial port. Serial protocols such as EIA-530, RS-449, V.35 and V.36 utilize higher speed differential channels for data and clock but use slower single ended channels for control and handshaking signals. Differential drivers and receivers require two conductors per signal to achieve faster speeds and greater signal integrity. Single ended use only one
This approach improves data rate and for the highest priority signals but minimizes cable and connector pinout.
but single ended requires only one plus a common return path. T

Tx/Rx Type	Used on which protocols?	Electrical Characteristics
V.11 (RS-422)	High priority (Category 1) signals in EIA-530, RS-449, V.36 and X.21	Differential driver and receiver +/- 2 Volt driver swing 200mV Receiver sensitivity
V.35	Defined for high priority (Category 1) signals in the V.35 protocol. Some newer “V.35” ports use V.11 signals instead	Differential driver and receiver +/- 550 millivolt driver swing 200mV Receiver sensitivity Tightly controlled impedance requires special driver and receiver termination
V.28	Used for all signals in RS-232 or V.24. Category II signals for V.35	Single ended driver and receiver Driver swing at least +/-5V, up to +/-15V Bi-polar signals (+ and – voltage) 3V receiver sensitivity
V.10 (RS-423)	Category II signals for EIA-530, RS-449, V.36, X.21, AppleTalk	Single ended driver and receiver Driver swing less than +/-6V Bi-polar signals (+ and – voltage) Receiver has similar electrical characteristics as V.11

The SP3508 can configure its driver and receiver electrical characteristics to accommodate any of these standard protocols.

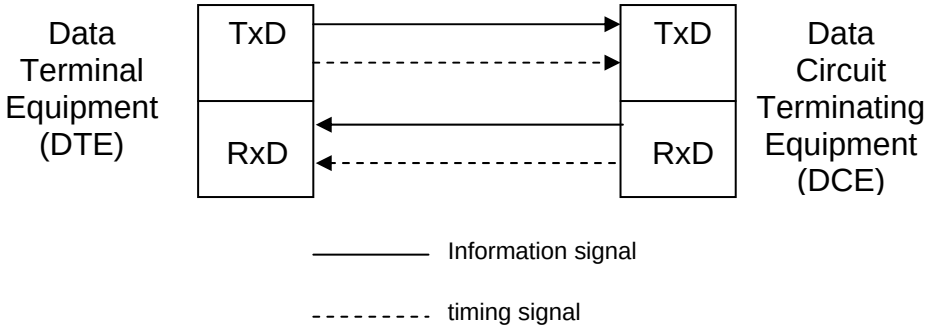
Proper termination for high speed signals in V.11 improves signal quality and bit error rate by eliminating reflections on the transmission line. The SP3508, SP508 and SP509 have V.11 receiver termination built into receivers 1, 2 and 3. Termination can be disabled using the TERM_OFF pin.

V.35 signals are specified for a tightly controlled source and receiver impedance. Therefore V.35 requires a termination network on both the driver and receiver. SP3508, SP508 and SP509 have V.35 receiver termination built into receivers 1, 2 and 3 and source termination built into receivers 1, 2 and 3. V.35 termination is active only when operating in V.35 mode (Mode 001) and can be disabled using the TERM_OFF pin.

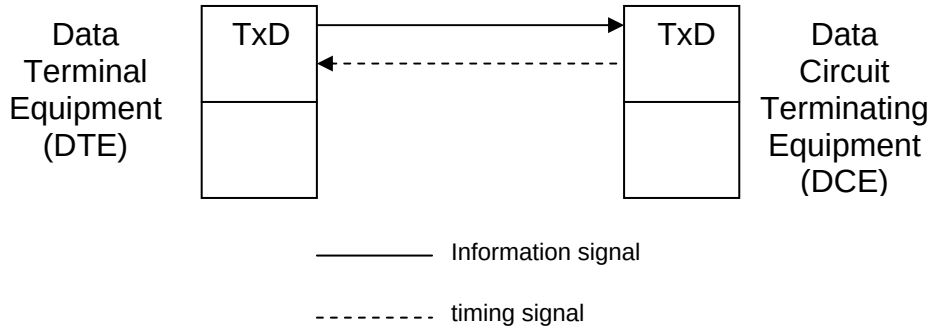
Clock Signals (Transmit Timing, Receive Timing)

Synchronous protocols require a clock reference signal. Timing signals may travel in the same direction as the data signals or they may originate only at the DCE, depending on protocol.

Co-Directional Timing: A configuration in which a timing signal and associated binary signals (data or control) are transferred in the same direction across the interface



Contra-Directional Timing: A configuration in which a timing signal and associated binary signals (data or control) are transferred in opposite directions across the interface. This configuration would apply to Transmit Clock/Data only.



Circuit Name	Timing		Timing Source	TIA/EIA Mnemonic	ITU-T Number
	Co	Contra			
Transmit Signal Element Timing		X	DCE	DB	114
Transmit Signal Element Timing	X		DTE	DA	113
Receiver Signal Element Timing	X		DCE	DD	115
Transmitted Data			DTE	BA	103
Received Data			DCE	BB	104

In the SCC-SP3508 connection example there are two drivers (T2, T3) and two receivers (R2, R3) reserved for clock signals. This allows the example system to support either co-directional or contra-directional clocks while acting as either the DTE or DCE.

All clock drivers or receivers are equipped with built in bus terminations to support high speed signals. In many protocols the clock frequency is run at twice the data rate, so having clean high speed timing is a must for reliable data transmission.

In CCITT (ITU) X.21bis there is only one clock signal provided by the DCE for both send and receive. If an X.21 DCE is connected to a DCE using another protocol, both the Transmit Clock and Receive Clock must be combined into one clocking signal.

Flow Control Signals

Clear To Send (CTS#) and Request To Send (RTS#)

These are used by the DTE (RTS) and DCE (CTS) to indicate if it is ready to accept data. Serial data is buffered on the SCC or UART before it is released to the CPU. RTS# and CTS# will stop the flow of data if the buffer is full to prevent buffer overflow and data loss. In a half-duplex bus RTS is sometimes used as a driver enable signal.

Handshake Signals

Data Terminal Ready and Data-Set Ready (DTR and DSR)

Data Terminal Ready and Data-Set Ready are held active whenever the terminal is powered on and functional (DTR) or when the modem (data set) is powered and active (DSR). However some communications protocols do toggle these signals during a communications session.

Modem Control Signals

Carrier Detect (DCD)

For a dial-up or other non-permanent channel, this signal indicates that a communications link is established. Carrier Detect is always directed from DCE to DTE. The QUICC-SCC has a Carrier Detect input. When operating as a DCE if Carrier Detect is required it can be driven using a general purpose output. On a dedicated line where a carrier connection is assured DCD can be driven together with DSR.

Test Mode, Local Loopback, Remote Loopback

The use of these signals is described in Bellcore specifications for Channel Service Units (CSU). They allow the telephone central office to put remote equipment into loopback modes to test the connection between the equipment and the central office switch. The test mode signal is driven from the remote equipment to indicate it is off-line in a test mode.

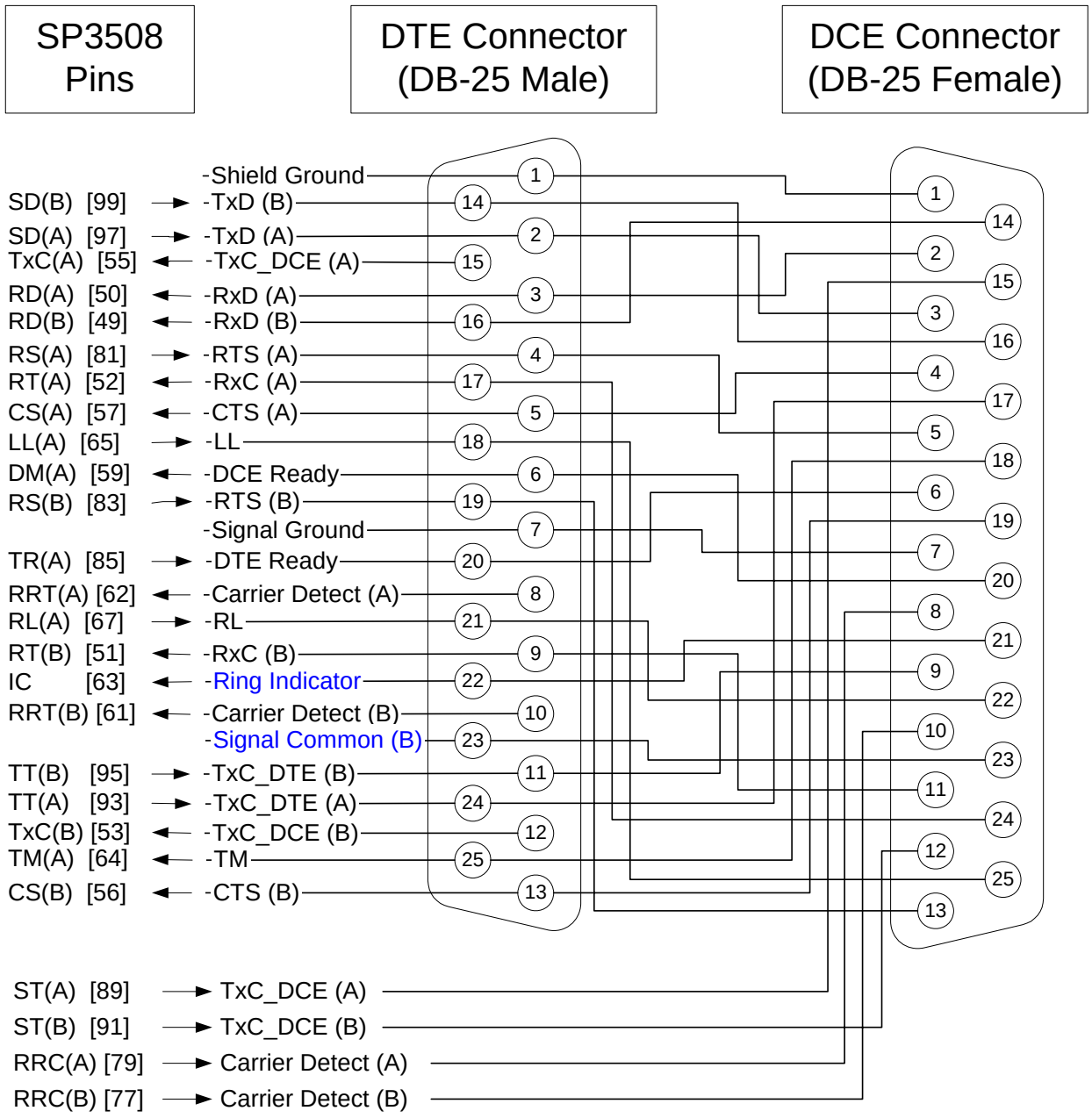
Ring Indicator

For a dial-up connection the Ring Indicator will toggle to alert the system to an incoming call. Typically this signal would be configured to trigger an interrupt to wake up the system and receive the call.

Note: all signals are referenced to signal names of the DTE. A QUICC SCC and SP3508 can be used to implement either a DCE or a DTE. For DCE, the pin functions will map to signal names complementary to DTE signal names. For example a DCE serial data out (SCC TxD pin) is mapped to the RxD pin on an external cable.

Example Connection for TIA/EIA-530-A

Also valid for RS-232 and V.35 on DB-25



The figure above shows the standard pin connections between SP3508 and the DB-25 connector specified in ANSI/TIA/EIA-530-A (1991). A male connector is specified for the DTE and a female connector for the DCE.

QUICC and SP3508 can easily support communication as either DTE or DCE. A simple way to enable this dual function is to use two external connectors, a male with DTE signals and a

female for DCE. All signals on the data cable are uni-directional. The signal routing in the figure above shows the proper “crossover” of signals for DTE-DCE operation.

Two signals deserve special consideration. Transmit Signal Element Timing (TxC) when provided by the DCE (contra-directional) is carried on pins 15 and 12. When provided by the DTE (co-directional) it is carried on pins 24 and 11. For the QUICC+SP3508 DTE TxC is an input to Receiver 3. For DCE the TxC is an output of Driver 3.

Carrier Detect is always provided by the DCE to the DTE. The DTE receiver input and DCE driver output are shown routed to the appropriate connectors.

It may also be possible to support both a DTE and DCE function from a single external connector. However this requires use of external cable-adapters to perform the signal cross-over and gender change. There are not enough pins available on the DB-25 to support both the DTE and DCE functions of TxC and Carrier Detect. To support both modes the input and output signals for TxC and Carrier Detect must share bi-directional pins. Driver enables STEN and RRCEN are active high, while receiver enables TxCEN# and RRTEN# are active low. The combined input to these four pins acts as a DCE/DTE select pin. Refer to figure 51 in the SP3508 datasheet.

RS-232 and V.24 also use this same DB-25 connector but with single-ended V.28 driver and receivers and different signal voltages. SP3508 has drivers and receivers that can be re-configured for either V.11/V.10 signal voltages (mode 100 = EIA-530-A) or V.28 voltage (mode 011 = RS-232/V.24). V.35 is also sometimes used with DB-25 connector instead of the bulkier M34 connector. SP3508 will also configure for the proper V.35 signal voltages (mode 001 = V.35). This flexibility allows QUICC+SP3508 to support all these operating modes using only a single SCC.

EIA-530-A is a modification of the original EIA-530 (1987) standard. The original is also supported by QUICC+SP3508 but will use different signals on pins 22 and 23 of the connector. Recommended signal connections for the SP3508 for EIA-530 (1987) and for other widely used protocols are shown in the tables below.

Cable Pinouts for SP3508 configured as a DTE

SP3508 Multiprotocol Configured as DTE

Interface to System Logic			Interface to Port-Connector	
Pin Number	Pin Mnemonic	Circuit	Pin Mnemonic	Pin Number
31	TxD	Driver_1	SD(A)	97
2	SDEN		SD(B)	99
32	TxCE	Driver_2	TT(A)	93
3	TTEN		TT(B)	95
33	ST	Driver_3	ST(A)	89
4	STEN		ST(B)	91
34	RTS	Driver_4	RS(A)	81
5	RSEN		RS(B)	83
35	DTR	Driver_5	TR(A)	85
6	TREN		TR(B)	87
36	DCD_DCE	Driver_6	RRC(A)	79
7	RRCEN		RRC(B)	77
37	RL	Driver_7	RL(A)	67
8	RLEN			
38	LL	Driver_8	LL(A)	65
9	LLEN#			
39	RxD	Receiver_1	RD(A)	50
10	RDEN#		RD(B)	49
40	RxC	Receiver_2	RT(A)	52
11	RTEN#		RT(B)	51
41	TxC	Receiver_3	TxC(A)	55
12	TxCEN#		TxC(B)	53
42	CTS	Receiver_4	CS(A)	57
13	CSEN#		CS(B)	56
43	DSR	Receiver_5	DM(A)	59
14	DMEN#		DM(B)	58
44	DCD_DTE	Receiver_6	RRT(A)	62
15	RRTEN#		RRT(B)	61
45	RI	Receiver_7	IC	63
16	ICEN#			
46	TM	Receiver_8	TM(A)	64
17	TMEN			
		Signal Ground		28, 60
		Frame Ground		

Recommended Signals and Port Pin Assignments

RS-232 or V.24 Mode 011			EIA-530 Mode 010 EIA-530A Mode 100			RS-449 and V.36 Mode 101			V.35, appendix II. Mode 001			X.21*bis* Mode 110			AppleTalk Mode 100		
Signal Type	Mnemonic	DB-25 Pin(M)	Signal Type	Mnemonic	DB-25 Pin(M)	Signal Type	Mnemonic	DB-37 Pin(M)	Signal Type	Mnemonic	M34 Pin(M)	Signal Type	Mnemonic	DB-15 Pin(M)	Signal Type	Mnemonic	DIN-8 Pin(F)
V.28	BA	2	V.11	BA(A)	2	V.11	SD(A)	4	V.35	103	P	V.11	T(A)	2	V.11	TxD -	3
			V.11	BA(B)	14	V.11	SD(B)	22	V.35	103	S	V.11	T(B)	9	V.11	TxD +	6
V.28	DA	24	V.11	DA(A)	24	V.11	TT(A)	17	V.35	113	U	V.11	X(A)	7**			
			V.11	DA(B)	11	V.11	TT(B)	35	V.35	113	W	V.11	X(B)	14**			
V.28	CA	4	V.11	CA(A)	4	V.11	RS(A)	7	V.28	105	C	V.11	C(A)	3			
			V.11	CA(B)	19	V.11	RS(B)	25				V.11	C(B)	10			
V.28	CD	20	V.11/10	CD(A)	20	V.11	TR(A)	12	V.28	108	H				V.10	HSKo	1
			V.11/Z	CD(B)	23	V.11	TR(B)	30									
V.28	RL	21	V.10	RL	21	V.10	RL	14	V.28	140	N						
V.28	LL	18	V.10	LL	18	V.10	LL	10	V.28	141	L						
V.28	BB	3	V.11	BB(A)	3	V.11	RD(A)	6	V.35	104	R	V.11	R(A)	4	V.11	RxD-	5
			V.11	BB(B)	16	V.11	RD(B)	24	V.35	104	T	V.11	R(B)	11	V.11	RxD+	8
V.28	DD	17	V.11	DD(A)	17	V.11	RT(A)	8	V.35	115	V						
			V.11	DD(B)	9	V.11	RT(B)	26	V.35	115	X						
V.28	DB	15	V.11	DB(A)	15	V.11	ST(A)	5	V.35	114	Y	V.11	S(A)	6			
			V.11	DB(B)	12	V.11	ST(B)	23	V.35	114	AA	V.11	S(B)	13			
V.28	CB	5	V.11	CB(A)	5	V.11	CS(A)	9	V.28	106	D	V.11	I(A)	5		GND	
			V.11	CB(B)	13	V.11	CS(B)	27				V.11	I(B)	12	V.10*	HSKi	2
V.28	CC	6	V.11/10	CC(A)	6	V.11	DM(A)	11	V.28	107	E	V.11	B(A)	7**	V.10	GPi	7
			V.11/Z	CC(B)	22	V.11	DM(B)	29				V.11	B(B)	14**			
V.28	CF	8	V.11	CF(A)	8	V.11	RR(A)	13	V.28	109	F						
			V.11	CF(B)	10	V.11	RR(B)	31									
V.28	CE	22							V.28	125	J						
V.28	TM	25	V.10	TM	25	V.10	TM	18	V.28	142	NN						
	AB	7		AB	7		SG	19		102	B		G	1		GND	4
		1			1			1			A						

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver

Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations

** X.21 use either B() or X(), not both

Cable Pinouts for SP3508 configured as a DCE

SP3508 Multiprotocol Configured as DCE

Interface to System Logic			Interface to Port-Connector	
Pin Number	Pin Mnemonic	Circuit	Pin Mnemonic	Pin Number
31	TxD	Driver_1	SD(A)	97
2	SDEN		SD(B)	99
32	TxCE	Driver_2	TT(A)	93
3	TTEN		TT(B)	95
33	ST	Driver_3	ST(A)	89
4	STEN		ST(B)	91
34	RTS	Driver_4	RS(A)	81
5	RSEN		RS(B)	83
35	DTR	Driver_5	TR(A)	85
6	TREN		TR(B)	87
36	DCD_DCE	Driver_6	RRC(A)	79
7	RRCEN		RRC(B)	77
37	RL	Driver_7	RL(A)	67
8	RLEN			
38	LL	Driver_8	LL(A)	65
9	LLEN#			
39	RxD	Receiver_1	RD(A)	50
10	RDEN#		RD(B)	49
40	RxC	Receiver_2	RT(A)	52
11	RTEN#		RT(B)	51
41	TxC	Receiver_3	TxC(A)	55
12	TxCEN#		TxC(B)	53
42	CTS	Receiver_4	CS(A)	57
13	CSEN#		CS(B)	56
43	DSR	Receiver_5	DM(A)	59
14	DMEN#		DM(B)	58
44	DCD_DTE	Receiver_6	RRT(A)	62
15	RRTEN#		RRT(B)	61
45	RI	Receiver_7	IC	63
16	ICEN#			
46	TM	Receiver_8	TM(A)	64
17	TMEN			
		Signal Ground		28, 60
		Frame Ground		

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver

Recommended Signals and Port Pin Assignments

RS-232 or V.24 Mode 011			EIA-530 Mode 010 EIA-530A Mode 100			RS-449 and V.36 Mode 101			V.35, app II. Mode 001			X.21*bis* Mode 110			AppleTalk Mode 100		
Signal Type	Mnemonic	DB-25 Pin(F)	Signal Type	Mnemonic	DB-25 Pin(F)	Signal Type	Mnemonic	DB-37 Pin(F)	Signal Type	Mnemonic	M34 Pin(F)	Signal Type	Mnemonic	DB-15 Pin(F)	Signal Type	Mnemonic	DIN-8 Pin(M)
V.28	BB	3	V.11	BB(A)	3	V.11	RD(A)	6	V.35	104	R	V.11	R(A)	4	V.11	RxD-	5
			V.11	BB(B)	16	V.11	RD(B)	24	V.35	104	T	V.11	R(B)	11	V.11	RxD+	8
V.28	DD	17	V.11	DD(A)	17	V.11	RT(A)	8	V.35	115	V						
			V.11	DD(B)	9	V.11	RT(B)	26	V.35	115	X						
V.28	DB	15	V.11	DB(A)	15	V.11	ST(A)	5	V.35	114	Y	V.11	S(A)	6			
			V.11	DB(B)	12	V.11	ST(B)	23	V.35	114	AA	V.11	S(B)	13			
V.28	CB	5	V.11	CB(A)	5	V.11	CS(A)	9	V.28	106	D	V.11	I(A)	5		GND	
			V.11	CB(B)	13	V.11	CS(B)	27				V.11	I(B)	12	V.10*	HSKi	2
V.28	CC	6	V.11	CC(A)	6	V.11	DM(A)	11	V.28	107	E	V.11	B(A)	7**	V.10	GPi	7
			V.11	CC(B)	22	V.11	DM(B)	29				V.11	B(B)	14**			
V.28	CF	8	V.11	CF(A)	8	V.11	RR(A)	13	V.28	109	F						
			V.11	CF(B)	10	V.11	RR(B)	31									
V.28	CE	22							V.28	125	J						
V.28	TM	25	V.10	TM	25	V.10	TM	18	V.28	142	NN						
V.28	BA	2	V.11	BA(A)	2	V.11	SD(A)	4	V.35	103	P	V.11	T(A)	2	V.11	TxD -	3
			V.11	BA(B)	14	V.11	SD(B)	22	V.35	103	S	V.11	T(B)	9	V.11	TxD +	6
V.28	DA	24	V.11	DA(A)	24	V.11	TT(A)	17	V.35	113	U	V.11	X(A)	7**			
			V.11	DA(B)	11	V.11	TT(B)	35	V.35	113	W	V.11	X(B)	14**			
V.28	CA	4	V.11	CA(A)	4	V.11	RS(A)	7	V.28	105	C	V.11	C(A)	3			
			V.11	CA(B)	19	V.11	RS(B)	25				V.11	C(B)	10			
V.28	CD	20	V.11	CD(A)	20	V.11	TR(A)	12	V.28	108	H				V.10	HSKo	1
			V.11	CD(B)	23	V.11	TR(B)	30									
V.28	RL	21	V.10	RL	21	V.10	RL	14	V.28	140	N						
V.28	LL	18	V.10	LL	18	V.10	LL	10	V.28	141	L						
	AB	7		AB	7		SG	19		102	B		G	1		GND	4
		1			1			1			A						

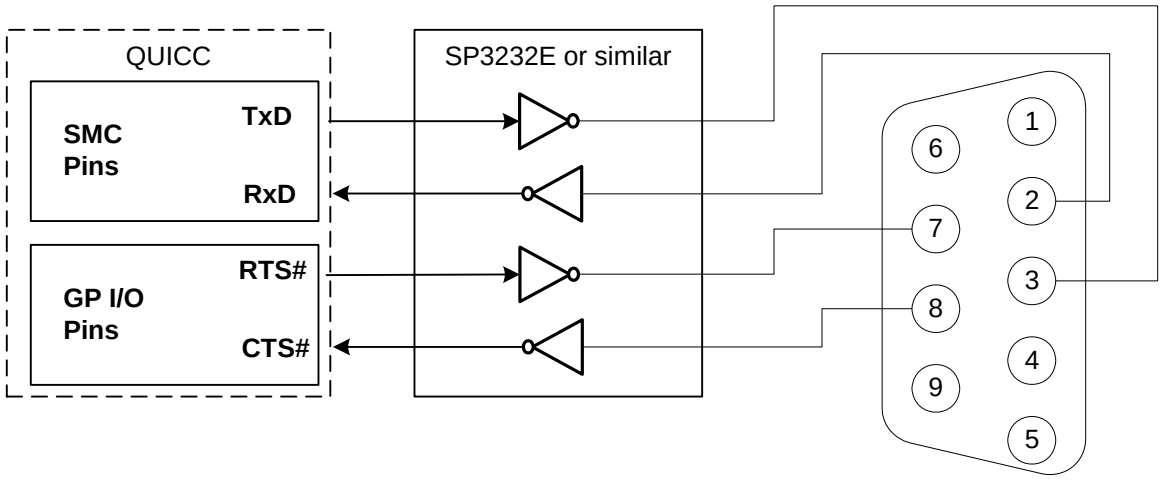
Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations

** X.21 use either B() or X(), not both

SMC - Maintenance and Configuration port

QUICC devices include one or more Serial Maintenance port Controllers (SMC). These are simplified serial ports used for diagnostic access, console or management ports. Each SMC has its own set of four dedicated pins (SMTxD, SMRxD, CLK and SMSYN). Additional signals are supported using general purpose pins.

SMC inputs and outputs are at CMOS voltages. A standard RS-232 transceiver such as the SP3232 can be used to drive SMC signals onto a DB-9 connector. The figure below shows a typical hookup for the SMC to be used with a standard VT100 style terminal or standard RS-232 connection.



If unused drivers and receivers are available on the SP3508, these may be used in place of a discrete RS-232 transceiver. All the drivers and receivers on the SP3508 can be enabled or disabled independently, allowing SMC and SCC functions to coexist on a shared SP3508.

Normally the SMC port should be operated with RS-232 (V.28) signal voltages. Signals on channels 7 and 8 are always in single-ended modes, either V.28 or V.10, or tri-state. V.10 driver outputs are compatible with RS-232. But care should be exercised if driving RS-232 signals into a V.10 receiver. The RS-232 specification allows signal voltage swing as high as +/-15V. If RS-232 signals are used to drive V.10 receivers you should ensure that the voltage swing seen at the receiver does not exceed +/-6V.