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MIGRATING FROM THE ST16C2550 TO THE XR16L2750

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1.0 INTRODUCTION

This application note describes the changes necessary and what to consider when migrating from the ST16C2550 to the XR16L2750.

1.1 HARDWARE DIFFERENCES

Table 1 below summarizes the differences between the ST16C2550 and XR16L2750.

TABLE 1: SUMMARY OF DIFFERENCES BETWEEN THE ST16C2550 AND XR16L2750

HARDWARE DIFFERENCES	ST16C2550	XR16L2750
Available Packages	48-pin TQFP, 44-pin PLCC and 40-pin PDIP	48-pin TQFP and 44-pin PLCC
Operating Voltage Range	2.97V - 5.5V	2.25V - 5.5V
5V Tolerant Inputs	No	Yes
Maximum data rate at 5V	4 Mbps	6.25 Mbps
Maximum data rate at 3.3V	1.875 Mbps	4 Mbps

- The ST16C2550 and XR16L2750 are both available in the 44-pin PLCC and 48-pin TQFP packages. The ST16C2550 is also available in the 40-pin PDIP package but the XR16L2750 is not.

- The ST16C2550 can operate from 2.97 V to 5.5V only. The XR16L2750 can operate from 2.25 V up to 5.5 V.

- The maximum data rate for the ST16C2550 is 4 Mbps at 5V using a 64 MHz external clock and 1.875 Mbps at 3.3V using a 30MHz external clock. The ST16C2550 uses a data sampling rate of 16X. The maximum data rate for the XR16L2750 is 6.25 Mbps at 5V using a 50 MHz external clock and 4 Mbps at 3.3V using a 33MHz external clock. These maximum data rates can be achieved for the XR16L2750 by enabling the 8X sampling rate via EMSR bit-7.

- In the 44-pin PLCC and 48-pin TQFP packages, the ST16C2550 and XR16L2750 have identical pinouts so they are fully pin-to-pin compatible. The XR16L2750 is not available in the 40-pin PDIP package.

1.2 FIRMWARE DIFFERENCES

The internal register set of the XR16L2750 is based on the internal register set of the ST16C2550, except that some unused bits in the ST16C2550 register set are used in the XR16L2750. Also, the XR16L2750 has an Enhanced Register Set not found in the ST16C2550. Table 2 on the following page lists the firmware differences between the ST16C2550 and XR16L2750.

TABLE 2: ST16C2550 AND XR16L2750 REGISTER SET DIFFERENCES

A2:A0	R/W	ST16C2550	XR16L2750
LCR Bit-7 = 0 (Standard Register Set)			
001	R/W	**Interrupt Enable Register (IER)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Not Used • Bit-4 = Not Used	**Interrupt Enable Register (IER)** • Bit-7 = Auto CTS# Interrupt Enable • Bit-6 = Auto RTS# Interrupt Enable • Bit-5 = Xoff Interrupt Enable • Bit-4 = Sleep Mode Enable
010	W	**FIFO Control Register (FCR)** • Bit-5 = Not Used • Bit-4 = Not Used	**FIFO Control Register (FCR)** • Bit-5 = TX FIFO Trigger Level Select Bit-1 • Bit-4 = TX FIFO Trigger Level Select Bit-0
010	R	**Interrupt Status Register (ISR)** • Bit-5 = Not Used • Bit-4 = Not Used	**Interrupt Status Register (ISR)** • Bit-5 = Auto RTS/CTS Interrupt • Bit-4 = Xoff or Special Character Interrupt
100	R/W	**Modem Control Register (MCR)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Not Used	**Modem Control Register (MCR)** • Bit-7 = BRG Prescaler Select • Bit-6 = IR Mode Enable • Bit-5 = XonAny
LCR Bit-7 = 0, FCTR Bit-6 = 1			
111	W	N/A	**Enhanced Mode Select Register (EMSR)** • 8X Sampling, LSR Interrupt Immediate, Auto RTS Hysteresis Select (MSB), RS485 Output Inversion, FLVL select - TX or RX FIFO
111	R	N/A	**FIFO Level Register (FLVL)** • Current Level of the TX or RX FIFO
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	N/A	**Device Revision (DREV)**
001	R	N/A	**Device ID (DVID) = 0x0A**
LCR = 0xBF (Enhanced Register Set)			
000	R	N/A	**FIFO Data Count Register (FC)**
000	W	N/A	**Trigger Level Register (TRG)** • Programmable Trigger Levels 1-64 for TX and RX FIFO
001	R/W	N/A	**Feature Control Register (FCTR)** • RX/TX Programmable Trigger Level Select, Scratchpad Swap, Trigger Table Select, Auto RS485 Enable, RX Infrared Input Inversion, Auto RTS Hysteresis Select (LSB)
010	R/W	N/A	**Enhanced Feature Register (EFR)** • Auto RTS/CTS Enable, Enable Enhanced (shaded) bits in Standard Register Set, Software Flow Control Select
100	R/W	N/A	**XON1**
101	R/W	N/A	**XON2**
110	R/W	N/A	**XOFF1**
111	R/W	N/A	**XOFF2**

1.3 REPLACING THE **ST16C2550** WITH THE **XR16L2750**

You can directly replace the ST16C2550 with the XR16L2750 in the 44-pin PLCC and 48-pin TQFP packages. In those packages, they are pin-to-pin compatible. If using the ST16C2550 in the 40-pin PDIP package, then hardware changes will be required since the XR16L2750 is not available in that package.

Since the internal registers of the XR16L2750 are the same as the ST16C2550, the XR16L2750 will work with the same driver that is used with the ST16C2550 without any changes. However, to take advantage of the enhanced features in the XR16L2750 such as the larger FIFO, Programmable Trigger Levels, FIFO Level Counters, Auto Hardware Flow Control, Auto Software Flow Control and RS-485 Half-Duplex Control, the existing software needs to be modified.

In a nutshell, the ST16C2550 and XR16L2750 are very similar devices but with different FIFO sizes and the XR16L2750 has some addtional features not found in the ST16C2550.

NOTICE