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EXAR'S XR16L784 COMPARED WITH OXFORD'S OX16C954

Author: PY

1.0 INTRODUCTION

This application note describes the hardware and firmware-related differences between Exar's XR16L784 with Oxford's OX16C954. The Exar and Oxford Quad UARTs are very different devices.

1.1 HARDWARE DIFFERENCES

- The XR16L784 is available in the smaller 64-pin TQFP package, while the OX16C954 is available in the 68-pin PLCC and 80-pin TQFP packages.
- Overall, the XR16L784 is simpler and more flexible to design with these three features:
  - The XR16L784 can operate from 2.95 to 5.5 V with 5 V tolerant inputs. The OX16C954 can operate at 5 V or 3.3 V, but it does not have 5 V tolerant inputs at 3.3 V operation.
  - The XR16L784 has a single chip select input pin and interrupt output pin for all 4 channels while the OX16C954 has individual chip select input pin and interrupt output pin for each channel.
  - The XR16L784 has a 16/68# input pin to select the device for Intel or Motorola data bus interface. The OX16C954 can operate only in the Intel data bus interface.

1.2 FIRMWARE DIFFERENCES

- The internal registers of the XR16L784 are much simpler than the internal registers of the OX16PCI954. The XR16L784 has a flat sequential register set while the OX16PCI954 has 3 levels of shadow registers. The XR16L784 uses 4 address lines to access the internal registers instead of the traditional 3 address lines therefore eliminating having to deal with shadow registers. The 16C550 Standard Register Set and the Enhanced Register Set can all be accessed from the same location. Note that the XR16L784 has more registers in the Enhanced Register Set than the OX16C954 has in its Enhanced Register Set. The OX16C954 has a Standard Register Set, Enhanced Register Set, Indexed Control Register Set and Additional Status Register Set. As long as the last value written to LCR was not 0xBF, the Index Control Register (ICR) is accessed by writing the desired address offset for the ICR to the Scratchpad register and then writing to the ICR. Note that this is for writing to the ICR only. To read from ICR, you must write to a bit in one of the Indexed Control Registers to enable reading from the ICR. The Additional Status Registers can only be read when another bit in the Indexed Control Registers is set.
- The XR16L784 has the ability to write to all channels simultaneously (via Device Configuration Register REG2 bit-0) for smaller and quicker initialization routines. Once simultaneous write has been enabled for the XR16L784, writing to any channel register will write to the same register of all channels. In the OX16C954, it is necessary to initialize each channel individually.
- The interrupt scheme of the XR16L784 and OX16C954 is similar to the interrupt scheme used in the industry standard 16C550 but the XR16L784 has some enhancements like the ability to clear one interrupt in each of the channels per interrupt service by reading the Global Interrupt Status Registers. The OX16C954 can only service one channel per interrupt service.
- In addition to Automatic RTS/CTS Hardware Flow Control, the XR16L784 also supports Automatic DTR/DSR Hardware Flow Control. This gives hardware designers flexibility in selecting which signals to use for hardware flow control. This feature is not available in the OX16C954.
- The XR16L784 has Automatic 2 character Xon/Xoff Software Flow Control. In Automatic 2 character Xon/Xoff Software Flow Control, two flow control characters (Xoff1, Xoff2, Xon1, Xon2) are sent at the appropriate times instead of just a single character. This is to ensure that the first character is not accidentally inter-

preted as a software flow control character if it was not meant to be. More importantly, it will allow the software routine to be able to use the entire character set including the Xon and Xoff characters as part of the data stream since they will not necessarily be interpreted as software flow control characters unless they are received one after another. The OX16C954 only has the Automatic 1 character Xon/Xoff Software Flow Control.

- The XR16L784 has an Automatic RS485 Half-Duplex Control with Turn-Around Delay. RTS# or DTR# output is a logic one while transmitting and becomes a logic zero after a specified delay indicated in MSR bits 7-4 following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote stations's response. The delay optimizes the time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver. This delay prevents undesirable line signal disturbance that causes signal degradation. The OX16C954 does not have the Turn-Around Delay feature.
- The XR16L784 has 16 selectable levels of RTS Hysteresis ranging from ±4 to ±52 when using programmable trigger levels (Table-D). For example if the RX Trigger Level was programmed for 32 bytes and the RTS Hysteresis was selected at ±20, the RTS# pin will not be forced to a logic 1 (RTS off) until the receive FIFO reaches 52 bytes. The RTS# pin will return to a logic 0 (RTS on) after the RX FIFO is unloaded to 12 bytes. The OX16C954 has a similar feature. For the OX16C954, the software driver has to manually select the upper level to halt transmission and the lower level to resume transmission independent of the RX Trigger Level. It is also up to the software driver to ensure that the upper level is greater than the lower level since the device does not perform that check.
- The OX16C954 can be programmed to operate in a wake-up mode for Multidrop applications. This feature is not available in the XR16L784.
- The OX16C954 can disable and enable the TX or RX output. This feature is not available in the XR16L784.
- The XR16L784 has a BRG prescaler of 1 or 4. The OX16C954 has a Baud Rate Generator Prescaler of 1 to 31.875.
- The XR16L784 has a Data Sampling Rate of 8X or 16X. The OX16C954 has a Data Sampling Rate of 4X to 16X.
- The XR16L784 has TX and RX FIFOs of 64 bytes deep and the OX16C954 has TX and RX FIFOs of 128 bytes deep.

1.3 REPLACING THE OX16C954 WITH THE XR16L784

The XR16L784 is a much simpler device to design than the OX16C954 because the XR16L784 has a single chip select input and interrupt output. Since it is able to do simultaneous writes to all the channels, the initialization of the XR16L784 is much easier and quicker than the OX16C954. With a Global Interrupt Source Register, data throughput is increased and multiple channels can be serviced per interrupt, reducing CPU bandwidth requirements. In addition to that, the XR16L784 has many enhanced features for increased performance that are not available in the OX16C954 as mentioned above in the Firmware Differences section.

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