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EXAR'S XR16C850 COMPARED WITH OXFORD'S OX16C950

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1.0 INTRODUCTION

This application note describes the major difference between Exar's XR16C850 with Oxford's OX16C950. These devices are very similar, with a few hardware, firmware-related and bus timing differences.

1.1 HARDWARE DIFFERENCES

- The Oxford OX16C950 and Exar XR16C850 are available in the 48-pin TQFP and 44-pin PLCC packages. Additionally, the XR16C850 is available in the 40-pin PDIP (for compatibility to early families) and 52-pin QFP packages.
- In the 48-pin TQFP package, the Exar and Oxford UARTs are pin-to-pin compatible if pin 36 is tied to VCC.
- In the 44-pin PLCC package, the Exar and Oxford UARTs are pin-to-pin compatible if pin 34 is tied to VCC.
- Here is a summary of the pin differences between the XR16C850 and OX16C950 and the changes that need to be made when replacing the OX16C950 with the XR16C850:

TABLE 1: PIN DIFFERENCES BETWEEN THE XR16C850 AND OX16C950

OX16C950 PIN NAME	XR16C850 PIN NAME	44-PLCC PIN NUMBER	48-TQFP PIN NUMBER	CHANGES/COMMENTS
N.C.	CLKSEL	N/A	13	No change necessary. CLKSEL pin on XR16C850 has internal pull-up.
CLKSEL	N.C.	23	21	No change necessary. CLKSEL function can be performed via internal register MCR bit-7 in the XR16C850.
N.C.	BUS8/16	N/A	25	No change necessary. BUS8/16 pin on XR16C850 has internal pull-up.
INTSEL#	SEL	34	36	Only pin-to-pin compatible if this pin is connected to VCC. If this pin is tied to GND, XR16C850 will be in PC Mode.
FIFOSEL	N.C.	1	37	No change necessary. OX16C950 selects FIFO depths of 16 or 128 byte FIFOs. XR16C850 FIFO depth is always 128 bytes.
VSEL	N.C.	N/A	48	No change necessary. XR16C850 can operate at 5 or 3.3 V in all packages. VSEL pin on OX16C950 selects between 5 and 3 V operation. OX16C950 in 44-pin PLCC package can only operate at 5 V.

- The XR16C850 can operate in both the Intel and PC Mode while the OX16C950 can only operate in the Intel Bus Mode.

1.2 BUS TIMING DIFFERENCES

- The OX16C950 requires that the -CS pin is asserted before the -IOR or -IOW pin at the beginning of the read/write cycle and the -IOR or -IOW pin must be de-asserted before the -CS pin is de-asserted at the end of the cycle. During a read, the Exar UART can have either the -CS or the -IOR signal asserted first and have either signal be de-asserted first. The signals are wire-ORed in the Exar UART, therefore the second signal asserted initiates the read cycle and the first signal de-asserted terminates the read cycle. The same is true during a write for -CS and -IOW. The flexibility of the Exar UARTs timing can be important in designs using DSP, ARM, and MIPS processors.

1.3 FIRMWARE DIFFERENCES

- The internal registers of the XR16C850 are much simpler than the internal registers of the OX16C950. The XR16C850 only has one level of shadow registers while the OX16C950 has 3 levels. The XR16C850 has the 16C550 Standard Register Set and the Enhanced Register Set. The Enhanced Register Set can be accessed by writing 0xBF to the LCR register. Note that the XR16C850 has more registers in the Enhanced Register Set than the OX16C950 has in their Enhanced Register Set. The OX16C950 has a Standard Register Set, Enhanced Register Set, Indexed Control Register Set and Additional Status Register Set. As long as the last value written to LCR was not 0xBF, the Index Control Register (ICR) is accessed by writing the desired address offset for the ICR to the Scratchpad register and then writing to the Index Control Register. Note that this is for writing to the Index Control Register only. To read from the Index Control Register, you must write to a bit in one of the Indexed Control Registers to enable reading from the Index Control Register. The Additional Status Registers can only be read when another bit in the Indexed Control Registers is set.
- The XR16C850 has Automatic 2 character Xon/Xoff Software Flow Control. In Automatic 2 character Xon/Xoff Software Flow Control, two flow control characters (Xoff1, Xoff2, Xon1, Xon2) are sent at the appropriate times instead of just a single character. This is to ensure that the first character is not accidentally interpreted as a software flow control character if it was not meant to be. More importantly, it will allow the software routine to be able to use the entire character set including the Xon and Xoff characters as part of the data stream since they will not necessarily be interpreted as software flow control characters unless they are received one after another. The OX16C950 only has the Automatic 1 character Xon/Xoff Software Flow Control.
- The XR16C850 and OX16C950 both have Automatic RS485 Half-Duplex Control that will automatically control the direction of the RS485 transceivers. The Automatic RS485 Half-Duplex Control is through the OP1# pin for the XR16C850 and through the RTS# pin for the OX16C950.
- The XR16C850 has 3 selectable levels of RTS Hysteresis ranging from ±4 to ±8 when programmable trigger levels (Table-D) are used. For example if the RX Trigger Level was programmed for 32 bytes and the RTS Hysteresis was selected at ±8, the RTS# pin will not be forced to a logic 1 (RTS off) until the receive FIFO reaches 40 bytes. The RTS# pin will return to a logic 0 (RTS on) after the RX FIFO is unloaded to 24 bytes. The OX16C950 has a similar feature. For the OX16C950, the software driver has to manually select the upper level to halt transmission and the lower level to resume transmission independent of the RX Trigger Level. It is also up to the software driver to ensure that the upper level is greater than the lower level since the device does not perform that check.
- The OX16C950 can be programmed to operate in a wake-up mode for Multidrop applications. This feature is not available in the XR16C850.
- The OX16C950 can disable and enable the TX or RX output. This feature is not available in the XR16C850.
- The XR16C850 has a BRG prescaler of 1 or 4. The OX16C950 has a Baud Rate Generator Prescaler of 1 to 31.875.
- The XR16C850 has a Data Sampling Rate of 16X. The OX16C950 has a Data Sampling Rate of 4X to 16X.

1.4 REPLACING THE OX16C950 WITH THE XR16C850

You can directly replace Oxford's OX16C950 with Exar's XR16C850 in the 48-TQFP or 44-PLCC package if the INTSEL# pin of the OX16C950 is tied to VCC as described previously in the Hardware Differences section. If using the XR16C850 in the other packages, hardware changes will be required since the OX16C950 is not available in those packages.

There should not be any timing problems replacing the OX16C950 with the XR16C850 because it is more flexible than the OX16C950 as described in the bus timing section.

The software will need to be updated to take advantage of the enhanced features of the XR16C850 that are not available in or different from the OX16C950.

In a nutshell, the XR16C850 and OX16C950 are available in similar packages and have similar features but the XR16C850 has a much simpler internal register set for faster and easier software development.