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EXAR'S XR16L2550 AND XR16L2551 COMPARED WITH TI'S TL16C752B

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1.0 INTRODUCTION

This application note describes the major difference between Exar's 2-channel UARTs (XR16L2550 and XR16L2551) with TI's TL16C752B. These devices are similar, with a few hardware, firmware-related and bus timing differences.

1.1 HARDWARE DIFFERENCES

- Here is a table of the different packages that are available for each device:

TABLE 1: AVAILABLE PACKAGES FOR THE XR16L2550, XR16L2551 AND TL16C752B

PACKAGE	XR16L2550	XR16L2551	TL16C752B
32-Pin QFN	YES	YES	NO
44-Pin PLCC	YES	NO	NO
48-Pin TQFP	YES	YES	YES

- Since the only package in common is the 48-pin QFP package, the following table shows pinout differences for the XR16L2550 and XR16L2551 with the TL16C752B in the 48-pin TQFP package:

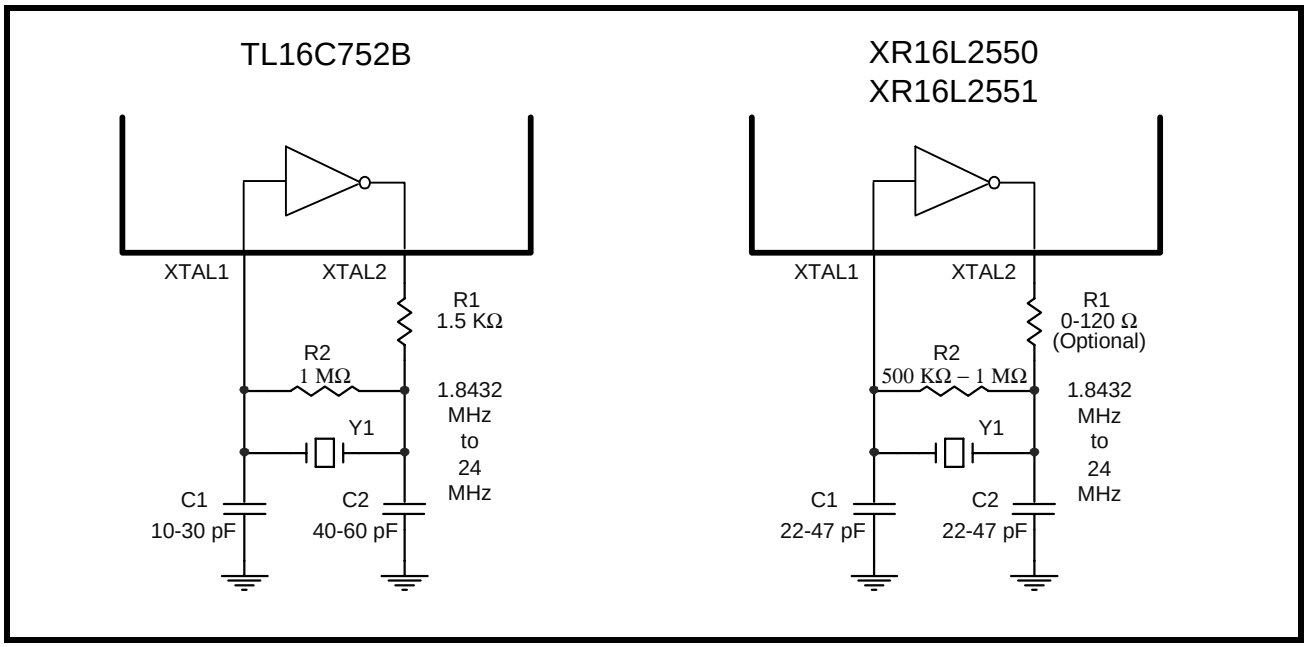
TABLE 2: PINOUT DIFFERENCES BETWEEN XR16L2550 AND XR16L2551 WITH TL16C752B IN 48-QFP PACKAGE

EXAR 2-CHANNEL UART	TI 2-CHANNEL UART	PINOUT DIFFERENCES
XR16L2550IM	TL16C752BPT	Fully Pin-to-pin compatible.
XR16L2551IM	TL16C752BPT	The XR16L2551 have 2 additional inputs where they are NC or "No Connects" on the TL16C752B: • Pin 12 (PwrSave): If not using sleep mode in the TL16C752B, this pin can be tied to VCC or GND. If sleep mode is used, this pin should be tied to GND for similar operation to the TL16C752B. If this pin is tied to VCC while sleep mode is enabled, the address, data and control lines will be isolated from the bus to further reduce the power consumption. Please see datasheet for complete details. • Pin 24 (16/68#): This pin should be tied to VCC so that it will operate in the Intel bus mode. The TL16C752B can only operate in this mode.

- Exar's 48-pin TQFP package is thinner (1.2 mm) than TI's 48-pin LQFP package (1.6 mm).

- The oscillator circuitry is similar and will operate in most cases, but there are some differences when using a crystal oscillator and when using an external clock. See Figure 1 for the differences in the oscillator circuitry for a crystal oscillator. When using an external clock input for frequencies greater than 24 MHz, Exar's 2-channel UARTs will require a 2K pull-up resistor on the XTAL2 pin.

FIGURE 1. CRYSTAL OSCILLATOR CIRCUITRY DIFFERENCES



1.2 BUS TIMING DIFFERENCES

- The TL16C752B requires that the -CS pin be asserted first before the -IOR or -IOW pin and the -IOR or -IOW pin must be de-asserted before the -CS pin is de-asserted. During a read, the Exar 2-channel UARTs can have either the -CS or the -IOR signal asserted first and have either signal be de-asserted first. The signals are wire-ORed in the Exar 2-channel UARTs, therefore the second signal asserted will initiate the read cycle and the first signal de-asserted terminates the read cycle. The same is true during a write for -CS and -IOW. The flexibility of the Exar 2-channel UARTs timing can be important in DSP, ARM, and MIPS designs. Also, because of this flexibility, the Exar 2-channel UARTs will work with the timing used for the TL16C752B.

1.3 Firmware Differences

1.3.1 Firmware Differences Between the XR16L2550 and TL16C752B

The internal registers in the XR16L2550 and TL16C752B are similarwith some exceptions:

Table 3: XR16L2550 and TL16C752B Register Set Differences

A2:A0	R/W	XR16L2550	TL16C752B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = Infrared Mode Enable • Bit-2 = Reserved (RI# during Internal Loop-back)	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	**Scratchpad Register (SPR)**	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	**Scratchpad Register (SPR)**	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A and B • Status Bits - RX FIFO level above RX Trigger Level for channels A and B

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.1.1 Summary of Differences Between the XR16L2550 and TL16C752B

Some differences between the XR16L2550 and TL16C752B are summarized in the table below.

TABLE 4: DIFFERENCES BETWEEN EXAR'S XR16L2550 WITH TI'S TL16C752B

COMPARISON	XR16L2550	TL16C752B
Data Bus Standard	Intel	Intel
Power Supply Operation	**2.25, 3.3 and 5 V**	3.3 V only
5 V Tolerant Inputs	**5 V Tolerant Inputs**	No
Max Operating Current	**1 mA @ 2.5 V** **1.3 mA @ 3.3 V** **3 mA @ 5 V**	20 mA @ 3.3 V
Max Frequency on XTAL1	**16 MHz @ 2.5 V** 30 MHz @ 3.3 V **50 MHz @ 5 V**	**48 MHz @ 3.3 V**
Data Sampling Rates	16X	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	**1 Mbps @ 2.5 V** 1.875 Mbps @ 3.3 V **3.125 Mbps @ 5 V**	3 Mbps @ 3.3 V
Package	48-TQFP, 44-PLCC, **32-QFN**	48-LQFP
Operating Temperature Ranges	Industrial	Commercial and Industrial
48-pin package thickness	**1.2 mm (TQFP)**	1.6 mm (LQFP)
TX/RX FIFO Size	16	**64**
TX/RX Trigger Tables	1 Trigger Table	**2 Trigger Tables**
TX/RX FIFO Interrupt Trigger Levels	4 Selectable	16 Selectable (TLR) 4 Selectable (TLR = 0)
Single FIFO Ready Status Register	No	**FIFO Ready Status Register**
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	Auto Xon/Xoff Flow Control	Auto Xon/Xoff Flow Control
Auto Hysteresis Level	Next Upper and Lower trigger level	16 Selectable Levels Select Upper and Lower Hysteresis Levels irrespective of trigger level
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	No
Sleep Mode	Sleep Mode with Auto Wake-up	Sleep Mode with Auto Wake-up
Diagnostic Modes	Local Loopback	Local Loopback

1.3.2 Firmware Differences Between the XR16L2551 and TL16C752B

The internal registers in the XR16L2551 and TL16C752B are similar but with some exceptions:

TABLE 5: XR16L2551 AND TL16C752B REGISTER SET DIFFERENCES

A2:A0	R/W	XR16L2551	TL16C752B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = Infrared Mode Enable • Bit-2 = Reserved (RI# during Internal Loop-back)	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	**Scratchpad Register (SPR)**	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	**Scratchpad Register (SPR)**	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A and B • Status Bits - RX FIFO level above RX Trigger Level for channels A and B

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.2.1 Summary of Differences Between the XR16L2551 and TL16C752B

Some differences between the XR16L2551 and TL16C752B are summarized in the table below.

TABLE 6: DIFFERENCES BETWEEN EXAR'S XR16L2551 WITH TI'S TL16C752B

COMPARISON	XR16L2551	TL16C752B
Data Bus Standard	**Intel and Motorola**	Intel
Power Supply Operation	**2.5, 3.3 and 5 V**	3.3 V only
5V Tolerant Inputs	**5V Tolerant Inputs**	No
Max Operating Current	**1 mA @ 2.5 V** **1.3 mA @ 3.3 V** **3 mA @ 5 V**	20 mA @ 3.3 V
Max Frequency on XTAL1	**16 MHz @ 2.5 V** 30 MHz @ 3.3 V **50 MHz @ 5 V**	**48 MHz @ 3.3 V**
Data Sampling Rates	16X	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	**1 Mbps @ 2.5 V at 8X** **1.875 Mbps @ 3.3 V at 8X** **3.125 Mbps @ 5 V at 8X**	3 Mbps @ 3.3 V
Package	48-TQFP, 32-QFN	48-LQFP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
48-QFP package thickness	**1.2 mm**	1.6 mm
TX/RX FIFO Size	64	64
TX/RX Trigger Tables	1 Trigger Table	**2 Trigger Tables**
TX/RX FIFO Interrupt Trigger Levels	4 Selectable	16 Selectable (TLR) 4 Selectable (TLR = 0)
Single FIFO Ready Status Register	No	**FIFO Ready Status Register**
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	Auto Xon/Xoff Flow Control	Auto Xon/Xoff Flow Control
Auto Hysteresis Level	Next Upper and Lower trigger level	16 Selectable Levels Select Upper and Lower Hysteresis Levels irrespective of trigger level
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	No
Sleep Mode	Sleep Mode with Auto Wake-up	Sleep Mode with Auto Wake-up
Powerdown Mode	**Power-Save Mode**	No
Diagnostic Modes	Local Loopback	Local Loopback

1.4 Replacing the TL16C752B with the XR16L2550 or XR16L2551

You can directly replace TI's TL16C752B with Exar's XR16L2550 with minimal hardware changes if using the 48-LQFP package. Also, you can replace the TL16C752B with the XR16L2551 if the two extra input pins are tied to GND or VCC appropriately as discussed in Table 2. The crystal oscillator circuitry will work in most cases, but it may be necessary to modify the oscillator circuitry as well.

The software may need to be updated if the existing design is using the Halt and Resume Transmission Levels of the TL16C752B since the XR16L2550 and XR16L2551 do not have that feature. Software updates are also needed if infrared mode of the Exar 2-channel UARTs are used since that feature is not available in the TL16C752B.

The TL16C752B is a 3.3 V device only, but can be replaced by any of the Exar 2-channel UARTs because they can operate from 2.25 V to 5.5 V. At any voltage, the Exar 2-channel UARTs have a lower power consumption than the TL16C752B.

There should not be any timing problems replacing the TL16C752B with the Exar 2-channel UARTs because they are more flexible than the TL16C752B as described in the bus timing section.

1.5 TL16C752B Known Deficiencies

The TL16C752B has two known deficiencies and are directly stated in TI's datasheet.

On page 12 of the TL16C752B's datasheet dated "December 1999 - Revised August 2000," TI gives a note advising not to write to Baud Rate Divisors DLL and DLH (DLM) while in sleep mode. Exar 2-channel UARTs do not have any such problems.

On page 22 of the TL16C752B datasheet, they describe a "timing error condition" in non-FIFO mode where the LSR and IIR (ISR) reports a data byte as available to read from the RHR, but there is no valid data ready to be read from the RHR. The Exar 2-channel UARTs do not have this problem in FIFO or non-FIFO mode.

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