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EXAR'S SINGLE CHANNEL UARTS COMPARED WITH TI'S TL16C550C

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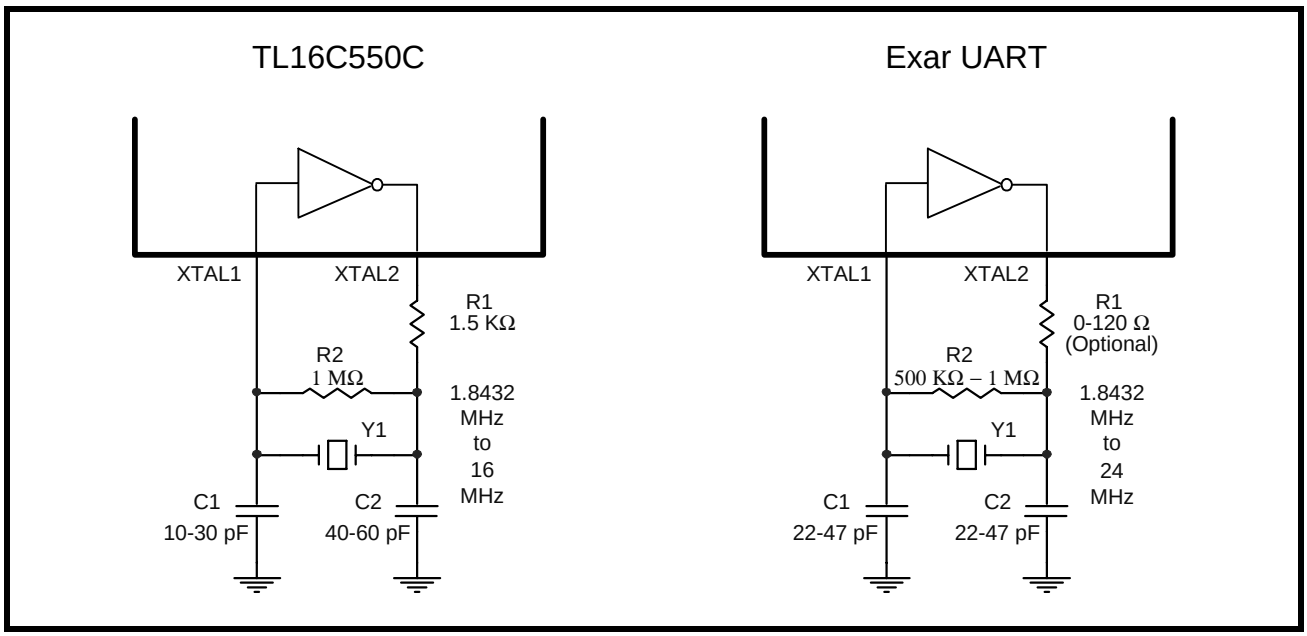
1.0 INTRODUCTION

This application note describes the major difference between Exar's ST16C550, ST16C580, ST16C650A, and XR16C850 with TI's TL16C550C. These devices are very similar, with a few hardware, bus timing and firmware-related differences.

1.1 HARDWARE DIFFERENCES

- The TI TL16C550C and Exar's ST16C550, ST16C580, ST16C650A and XR16C850 are all available in the 48-pin TQFP, 44-pin PLCC, and 40-pin PDIP packages. Additionally, the XR16C850 is available in the 52-pin QFP package. The Exar and TI UARTs are pin-to-pin compatible in the 40-pin PDIP package. In the 48-pin TQFP and 44-pin PLCC packages, the Exar and TI UARTs are pin-to-pin compatible if pin 34 of the ST16C650A and XR16C850 is tied to VCC (pin 34 of the TL16C550C, ST16C550, ST16C580 are not used).
- The oscillator circuitry is similar, but there are some differences when using a crystal oscillator and when using an external clock. See Figure 1below for the differences in the oscillator circuitry for a crystal oscillator. When using an external clock input for frequencies greater than 24 MHz, the Exar UARTs will require a 2K pull-up resistor on the XTAL2 pin.

FIGURE 1. CRYSTAL OSCILLATOR CIRCUITRY DIFFERENCES



1.2 BUS TIMING DIFFERENCES

- The TL16C550C requires that the -CS pin is asserted first before the -IOR or -IOW pin and the -IOR or -IOW pin must be de-asserted before the -CS pin is de-asserted. During a read, the Exar UART can have either the -CS or the -IOR signal asserted first and have either signal be de-asserted first. The signals are wire-ORed in the Exar UART, therefore the second signal asserted will initiate the read cycle and the first signal de-asserted terminates the read cycle. The same is true during a write for -CS and -IOW. The flexibility of the Exar UART timing can be important in DSP, ARM, and MIPS designs.

1.3 Firmware Differences

1.3.1 Firmware Differences Between the TL16C550C and ST16C550

The internal registers in the TL16C550C and ST16C550 are similar but with some exceptions:

Table 1: ST16C550 and TL16C550C Register Set Differences

A2:A0	R/W	ST16C550	TL16C550C
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-5 = Not Used	**Modem Control Register (MCR)** • Bit-5 = Auto RTS/CTS Flow Control Enable

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.2 Summary of Differences Between the ST16C550 and TL16C550C

The differences between the ST16C550 and TL16C550C is summarized in the table below.

Table 2: Differences Between Exar's ST16C550 with TI's TL16C550C

Comparison	ST16C550	TL16C550C
Data Bus Standard	Intel	Intel
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**1.3 mA @ 3.3 V** **3 mA @ 5 V**	8 mA @ 3.3 V 10 mA @ 5 V
Max Frequency on XTAL1	**16 MHz @ 3.3 V** **24 MHz @ 5 V**	14 MHz @ 3.3 V 16 MHz @ 5 V
Data Sampling Rates	16X	16X
BRG Prescaler	1	1
Max Data Rate	**1 Mbps @ 3.3 V** **1.5 Mbps @ 5 V**	875 Kbps @ 3.3 V 1 Mbps @ 5V
Package	44-PLCC, 48-TQFP, 40-PDIP	44-PLCC, 48-TQFP, 40-PDIP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
TX/RX FIFO Size	16	16
TX/RX Trigger Tables	1 Trigger Table	1 Trigger Table
TX FIFO Interrupt Trigger Levels	1	1
RX FIFO Interrupt Trigger Levels	4 Selectable	4 Selectable
Hardware Flow Control	N/A	**Auto RTS/CTS Flow Control**
Software Flow Control	N/A	N/A
Infrared Mode	N/A	N/A
Sleep Mode	N/A	N/A
Low Power Mode	N/A	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	N/A	N/A

1.3.3 Firmware Differences Between the TL16C550C and ST16C580

The internal registers in the TL16C550C and ST16C580 are similar but with some exceptions:

TABLE 3: ST16C580 AND TL16C550C REGISTER SET DIFFERENCES

A2:A0	R/W	ST16C580	TL16C550C
LCR Bit-7 = 0			
001	R/W	**Interrupt Enable Register (IER)** • Bit-7 = Auto CTS# Interrupt Enable • Bit-6 = Auto RTS# Interrupt Enable • Bit-5 = Xoff Interrupt Enable • Bit-4 = Sleep Mode Enable	**Interrupt Enable Register (IER)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Not Used • Bit-4 = Not Used
010	W	**FIFO Control Register (FCR)** • Bit-5 = TX FIFO Trigger Level Select Bit-1 • Bit-4 = TX FIFO Trigger Level Select Bit-0	**FIFO Control Register (FCR)** • Bit-5 = Not Used • Bit-4 = Not Used
010	R	**Interrupt Status Register (ISR)** • Bit-5 = Auto RTS/CTS Interrupt • Bit-4 = Xoff or Special Character Interrupt	**Interrupt Status Register (ISR)** • Bit-5 = Not Used • Bit-4 = Not Used
100	R/W	**Modem Control Register (MCR)** • Bit-7 = BRG Prescaler Select • Bit-6 = IR Mode Enable • Bit-5 = Not Used	**Modem Control Register (MCR)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Auto RTS/CTS Flow Control Enable
LCR = 0xBF			
010	R/W	**Enhanced Feature Register (EFR)** • Auto RTS/CTS Enable, Enhanced Functions Enable, Software Flow Control Select	N/A
100	R/W	**XON1**	N/A
101	R/W	**XON2**	N/A
110	R/W	**XOFF1**	N/A
111	R/W	**XOFF2**	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.3.1 Summary of Differences Between the ST16C580 and TL16C550C

The differences between the ST16C580 and TL16C550C is summarized in the table below.

TABLE 4: DIFFERENCES BETWEEN EXAR'S ST16C580 WITH TI'S TL16C550C

COMPARISON	ST16C580	TL16C550C
Data Bus Standard	Intel	Intel
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**1.3 mA @ 3.3 V** **3 mA @ 5 V**	8 mA @ 3.3 V 10 mA @ 5 V
Max Frequency on XTAL1	**8 MHz @ 3.3 V** **24 MHz @ 5 V**	14 MHz @ 3.3 V 16 MHz @ 5 V
Data Sampling Rates	16X	16X
BRG Prescaler	1 or 4	1
Max Data Rate	500 Kbps @ 3.3 V **1.5 Mbps @ 5 V**	**875 Kbps @ 3.3 V** 1 Mbps @ 5V
Package	44-PLCC, 48-TQFP, 40-PDIP	44-PLCC, 48-TQFP, 40-PDIP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
TX/RX FIFO Size	16	16
TX/RX Trigger Tables	1 Trigger Table	1 Trigger Table
TX FIFO Interrupt Trigger Levels	**4 Selectable**	1
RX FIFO Interrupt Trigger Levels	4 Selectable	4 Selectable
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	**Auto Xon/Xoff Flow Control**	N/A
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	**Sleep Mode with Auto Wake-up**	N/A
Low Power Mode	N/A	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	N/A	N/A

1.3.4 Firmware Differences Between the TL16C550C and ST16C650A

The internal registers in the ST16C650A offers more features than the TL16C550C with these differences:

TABLE 5: ST16C650A AND TL16C550C REGISTER SET DIFFERENCES

A2:A0	R/W	ST16C650A	TL16C550C
LCR Bit-7 = 0			
001	R/W	**Interrupt Enable Register (IER)** • Bit-7 = Auto CTS# Interrupt Enable • Bit-6 = Auto RTS# Interrupt Enable • Bit-5 = Xoff Interrupt Enable	**Interrupt Enable Register (IER)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Not Used
010	W	**FIFO Control Register (FCR)** • Bit-5 = TX FIFO Trigger Level Select Bit-1 • Bit-4 = TX FIFO Trigger Level Select Bit-0	**FIFO Control Register (FCR)** • Bit-5 = Not Used • Bit-4 = Not Used
010	R	**Interrupt Status Register (ISR)** • Bit-5 = Auto RTS/CTS Interrupt • Bit-4 = Xoff or Special Character Interrupt	**Interrupt Status Register (ISR)** • Bit-5 = Not Used • Bit-4 = Not Used
100	R/W	**Modem Control Register (MCR)** • Bit-7 = BRG Prescaler • Bit-6 = Infrared Mode Enable • Bit-5 = INT Type Select • Bit-3 = OP2 Control/INT Output Enable in PC Mode	**Modem Control Register (MCR)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Auto RTS/CTS Flow Control Enable • Bit-3 = OP2 Control
101	W	**Extra Feature Register (XFR)** • RS485 Output Inversion, XonAny, LSR Interrupt Immediate, RS485 Enable, IR RX Inversion, IR Half-Duplex/Full-Duplex Mode	N/A
110	W	**Infrared Transmit Pulsewidth Control Register (IRPW)**	N/A
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	**Device Revision (DREV)**	N/A
001	R	**Device ID (DVID)**	N/A
LCR = 0xBF			
010	R/W	**Enhanced Feature Register (EFR)** • Auto RTS/CTS Enable, Enhanced Functions Enable, Software Flow Control Select	N/A
100	R/W	**XON1**	N/A
101	R/W	**XON2**	N/A
110	R/W	**XOFF1**	N/A
111	R/W	**XOFF2**	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.4.1 Summary of Differences Between the ST16C650A and TL16C550C

The differences between the ST16C650A and TL16C550C is summarized in the table below.

TABLE 6: DIFFERENCES BETWEEN EXAR'S ST16C650A WITH TI'S TL16C550C

COMPARISON	ST16C650A	TL16C550C
Data Bus Standard	**Intel and PC Mode**	Intel
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**1.3 mA @ 3.3 V** **3 mA @ 5 V**	8 mA @ 3.3 V 10 mA @ 5 V
Max Frequency on XTAL1	**33 MHz @ 3.3 V** **50 MHz @ 5 V**	14 MHz @ 3.3 V 16 MHz @ 5 V
Data Sampling Rates	16X	16X
BRG Prescaler	**1 or 4**	1
Max Data Rate	**2 Mbps @ 3.3 V** **3.125 Mbps @ 5 V**	875 Kbps @ 3.3 V 1 Mbps @ 5V
Package	44-PLCC, 48-TQFP, 40-PDIP	44-PLCC, 48-TQFP, 40-PDIP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
TX/RX FIFO Size	**32**	16
TX/RX Trigger Tables	1 Trigger Table	1 Trigger Table
TX FIFO Interrupt Trigger Levels	**4 Selectable**	1
RX FIFO Interrupt Trigger Levels	4 Selectable	4 Selectable
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	**Auto Xon/Xoff Flow Control**	N/A
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	**Sleep Mode with Wake-up Indicator via an interrupt**	N/A
Low Power Mode	N/A	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	**Auto RS485 Mode**	N/A

1.3.5 Firmware Differences Between the TL16C550C and XR16C850

The internal registers in the TL16C550C and XR16C850 are similar but with some exceptions:

TABLE 7: XR16C850 AND TL16C550C REGISTER SET DIFFERENCES

A2:A0	R/W	XR16C850	TL16C550C
LCR Bit-7 = 0			
001	R/W	**Interrupt Enable Register (IER)** • Bit-7 = Auto CTS# Interrupt Enable • Bit-6 = Auto RTS# Interrupt Enable • Bit-5 = Xoff Interrupt Enable	**Interrupt Enable Register (IER)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Low Power Mode
010	W	**FIFO Control Register (FCR)** • Bit-5 = TX FIFO Trigger Level Select Bit-1 • Bit-4 = TX FIFO Trigger Level Select Bit-0	**FIFO Control Register (FCR)** • Bit-5 = 64 Byte FIFO Enable • Bit-4 = Not Used
010	R	**Interrupt Status Register (ISR)** • Bit-5 = Auto RTS/CTS Interrupt • Bit-4 = Xoff or Special Character Interrupt	**Interrupt Status Register (ISR)** • Bit-5 = 64 Byte FIFO Enabled • Bit-4 = Not Used
100	R/W	**Modem Control Register (MCR)** • Bit-7 = BRG Prescaler • Bit-6 = IR Mode Enable • Bit-5 = XonAny • Bit-3 = OP2 Control/INT Output Enable in PC Mode • Bit-2 = OP1 Control/Auto RS485 Enable	**Modem Control Register (MCR)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Auto RTS/CTS Flow Control Enable • Bit-3 = OP2 Control • Bit-2 = OP1 Control
LCR Bit-7 = 0, FCTR Bit-6 = 1			
111	W	**Enhanced Mode Select Register (EMSR)** • RX/TX DMA Select, FLVL select - TX or RX FIFO	N/A
111	R	**FIFO Level Register (FLVL)** • Current Level of the TX or RX FIFO	N/A
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	**Device Revision (DREV)**	N/A
001	R	**Device ID (DVID)**	N/A
LCR = 0xBF			
000	R	**FIFO Data Count Register (FC)**	N/A
000	W	**Trigger Level Register (TRG)** • Programmable Trigger Levels 1-64 for TX and RX FIFO	N/A
001	R/W	**Feature Control Register (FCTR)** • RX/TX Programmable Trigger Level Select, Scratchpad Swap, Trigger Table Select, Auto RS485 Enable, RX IR Input Inversion, Auto RTS Hysteresis Select (LSB)	N/A
010	R/W	**Enhanced Feature Register (EFR)** • Auto RTS/CTS Enable, Enhanced Functions Enable, Software Flow Control Select	N/A
100	R/W	**XON1**	N/A
101	R/W	**XON2**	N/A
110	R/W	**XOFF1**	N/A
111	R/W	**XOFF2**	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.5.1 Summary of Differences Between the XR16C850 and TL16C550C

The differences between the XR16C850 and TL16C550C is summarized in the table below.

TABLE 8: DIFFERENCES BETWEEN EXAR'S XR16C850 WITH TI'S TL16C550C

COMPARISON	XR16C850	TL16C550C
Data Bus Standard	**Intel and PC Mode**	Intel
Device ID and Revision	**Device ID and Revision**	
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**2.7 mA @ 3.3 V** 4 mA @ 5 V	8 mA @ 3.3 V 10 mA @ 5 V
Max Frequency on XTAL1	**22 MHz @ 3.3 V** **33 MHz @ 5 V**	14 MHz @ 3.3 V 16 MHz @ 5 V
Data Sampling Rates	16X	16X
BRG Prescaler	**1 or 4**	1
Max Data Rate	**1.375 Mbps @ 3.3 V** **2 Mbps @ 5 V**	875 Kbps @ 3.3 V 1 Mbps @ 5V
Package	44-PLCC, 48-TQFP, 40-PDIP, 52-QFP	44-PLCC, 48-TQFP, 40-PDIP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
TX/RX FIFO Size	**128**	16
TX/RX Trigger Tables	**4 Trigger Tables**	1 Trigger Table
TX FIFO Interrupt Trigger Levels	**Programmable (Table D)** **4 Selectable (Tables A-C)**	1
RX FIFO Interrupt Trigger Levels	**Programmable (Table D)** **4 Selectable (Tables A-C)**	4 Selectable
TX/RX FIFO Counters	**TX/RX FIFO Counters**	N/A
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	**Auto Xon/Xoff Flow Control**	N/A
Auto Hysteresis Level	**16 Selectable Levels**	N/A
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	**Sleep Mode with Auto Wake-up**	N/A
Low Power Mode	N/A	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	**Auto RS485 Mode**	N/A
Direct Memory Access Mode	**Direct Memory Access Mode (52-QFP)**	N/A
16-Bit Bus Mode	**16-Bit Bus Mode (52-QFP)**	N/A

1.4 REPLACING THE TL16C550C WITH THE ST16C550, ST16C580, ST16C650A OR XR16C850

You can directly replace TI's TL16C550C with Exar's ST16C550, ST16C580, ST16C650A or XR16C850 with minimal hardware changes if using the 48-TQFP, 44-PLCC or 40-PDIP packages. The same crystal oscillator circuitry should work in most cases, but it may be necessary to modify the oscillator circuitry as shown in Figure 1. If replacing with the XR16C850 in the 52-QFP package, hardware changes will be required since the TL16C550C is not available in that package.

Replacing the TL16C550C with the ST16C550 is simple when the system is not using Automatic RTS/CTS Hardware Flow Control.

When replacing the TL16C550C with the ST16C580, the software will need to be modified since Automatic RTS/CTS Hardware Flow Control is enabled differently for each UART. Also, the ST16C580 has some enhanced features that the TL16C550C does not like Automatic Xon/Xoff Software Flow Control, Sleep Mode and Infrared Mode.

When replacing the TL16C550C with the ST16C650A or XR16C850, the software will need to be modified since Automatic RTS/CTS Hardware Flow Control is enabled differently for each UART. And it would also need to be updated in order to take advantage of the enhanced features of the ST16C650A and XR16C850 that are not available in the TL16C550C.

There should not be any timing problems replacing the TL16C550C with the ST16C550, ST16C580, ST16C650A or XR16C850 because they are more flexible than the TL16C550C as described in the bus timing section.