XRP772X Current Measurement Application Note

GENERAL DESCRIPTION

The Power^{XR} XRP772X has an enhanced current measurement function over the first generation Power^{XR} devices. With this enhancement it now becomes possible to do improved current measurement across the entire load range. This application note will discuss how to get the best accuracy out of the analog to digital current measurements.

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APPLICATION NOTE

DESCRIPTION OF ANALOG FRONT END

The XRP772X family has the following analog front end (AFE) for sampling current measurement.

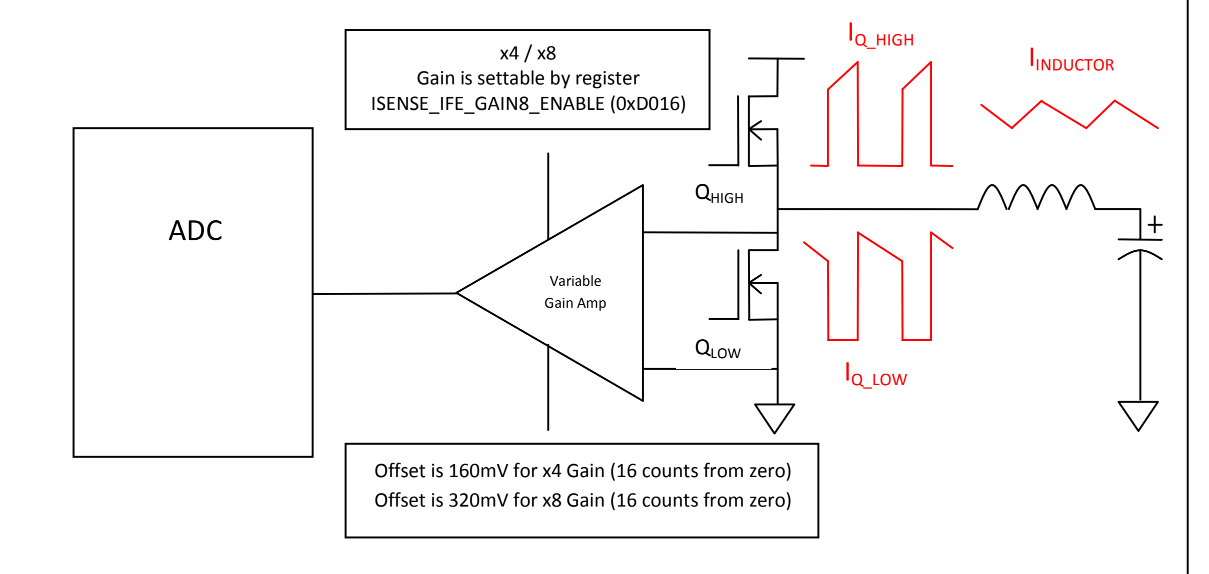

Figure 1 - Block Diagram of Analog Front End (AFE)

This analog to digital converter (ADC) is sampling once per switching cycle at a point approximately 100nsec before the end of the period as seen in Figure 2. This corresponds to just before the lowest point in the valley current waveform through the inductor. Another way of looking at it is that the current is sampled just before the low side MOSFET (Q_{LOW}) turns off.

The measurement that is being sampled is the voltage drop across the R_{dsOn} of Q_{LOW}. Hence, it's worth noting that the measurement taken is a negative voltage relative to GND since current is typically travelling from GND to LX.

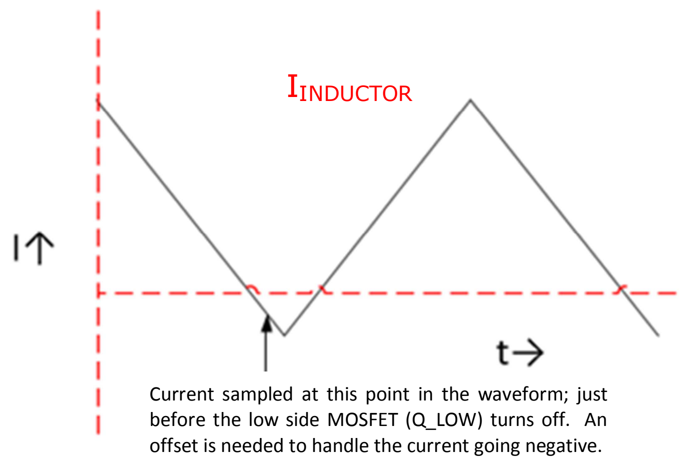

Figure 2 - Sampling of Current Waveform through Inductor

FORMULA FOR CONVERSION

Theory of Operation

The XRP772X uses a variable gain amplifier with an offset as an analog input stage into the ADC.

- The options for IFE_GAIN are 4 and 8.
- The corresponding V_{offset} is 160mV and 320mV respectively.

This offset is vital to getting a valid signal even at zero load when the valley current has reversed. During that event the measured voltage becomes a positive value and would have gone out of range without such an offset.

The XRP772X uses the following formula to generate it's ADC_OUTPUT for current measurement across the low side MOSFET.

$$ADC\_OUTPUT = {\left(IFE\_GAIN * \left(40mV + \left(V_{PGND} - V_{LX}\right)\right)\right)} \Big/ {10mV} \qquad (1)$$

The maximum value of ADC_OUTPUT is 128.

- When the IFE_GAIN is set to 4 the maximum ADC current sense range across the MOSFET *(V_{PGND}-V_{LX})* is -280mV to 40mV.
- When the IFE_GAIN is set to 8 the maximum ADC current sense range across the MOSFET *(V_{PGND}-V_{LX})* is -120mV to 20mV.

From this information we can conclude that an IFE_GAIN setting of 8 is best chosen for lower current designs where higher R_{dsOn} MOSFETs are used for Q_{LOW}. This leaves an IFE_GAIN setting of 4 as best for higher current designs where lower R_{dsOn} MOSFETs are used for Q_{LOW}.

Interrogating the XRP772X to Gather Telemetry

The content of the ADC_OUTPUT measurement for each channel can be queried via the IIC bus using the API call described in ANP-38. The method described is to use the I2C Peak/Poke utility under the Tools menu to:

- Read Bits [6:0] that are returned from the PWR_READ_CURRENT_CH0/1/2/3 API call (0x16, 0x,17, 0x18, and 0x19 respectively).

As discussed already, the returned value will represent a measured voltage with an applied offset and gain. The PowerArchitect™ software will choose the best IFE_GAIN setting for each channel based on the input current load levels and MOSFET R_{dsOn} data. To see what PowerArchitect™ has chosen use the I2C Peak/Poke utility to:

- Read the ISENSE_IFE_GAIN8_ENABLE register at 0xD016. This is a 4 bit register. Bits [3:0] correspond to their matching channel number. When the bit is set it is configured with an IFE_GAIN of 8. When not set an IFE_GAIN of 4 is configured.

Now all parameters to solve Equation (1) are available as chosen by PowerArchitect™. However, the IFE_GAIN value can be changed if determined necessary. For design review diligence the best method to check what IFE_GAIN to use for each channel is to determine the measurement bounds.

For the upper bound, we consider over current protection. Start with calculating the needed ADC value for OCP.

$$I_{Peak-Peak-Ripple} = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{(V_{IN} * F_{SW} * L)} \quad (2)$$

$$(V_{PGND} - V_{LX}) = \left(I_{OCP} - \frac{I_{Peak-Peak-Ripple}}{2} \right) * R_{dsON\_QLOW} \quad (3)$$

If Equation (3) > -120mV, then IFE_GAIN = 4, else IFE_GAIN = 8 (4)

For the lower bound, we consider low range current measurement accuracy. For this the positive current sense range should be checked. This is done the same way as the upper bound, but we will substitute I_{LOAD} = 0 for I_{OCP}.

$$(V_{PGND} - V_{LX}) = \left(I_{LOAD} - \frac{I_{Peak-Peak-Ripple}}{2} \right) * R_{dsON\_QLOW} \quad (5)$$

If Equation (5) > 20mV, then IFE_GAIN = 4, else IFE_GAIN=8 (6)

As an explanation, if the calculated $(V_{PGND}$-$V_{LX})$ signal at zero load exceeds 20mV, then it may be desirable to set the IFE_GAIN to 4 to take advantage of the 40mV positive range described in the first part of this document under Formula for Conversion. Otherwise, the best IFE_GAIN setting is 8.

Compute the Valley of the Ripple Current

To determine what the measured valley ripple current is the ADC_OUTPUT equation can be rearranged to solve for V_{PGND}-$V_{LX,}$ then divided by Q_{LOW} R_{dsOn}.

$$(V_{PGND} - V_{LX}) = \frac{(10mV * ADC\_OUTPUT)}{IFE\_GAIN} - 40mV \quad (7)$$

$$I_{VALLEY} = \frac{(V_{PGND} - V_{LX})}{R_{dsON\_QLOW}} \quad (8)$$

Better Implementation for Accurate Current Reporting

The entirety of this information was presented so that users would have an academic understanding of the mechanism of current measurement. The practical goal however is to describe the easiest way possible to measure output current. Ideally this should be identical with either the PowerArchitect™ dashboard or with custom code. To this end we will now introduce two new parameters. The first is K_R. K_R is a slope correction constant that will be multiplied into the MOSFET R_{dsON_QLOW} value to adjust the slope of the measured data. The second is K_O. K_O is an offset constant that will be applied to the final measured data in order to zero it out at the origin.

By adding KR and KO the process of arriving at a true output current measurement is achievable without having to worry about the fine details of duty cycle, inductance, frequency, and voltage. Equation (8) is modified as follows.

$$I_{OUT} = \frac{(V_{PGND} - V_{LX})}{R_{dsON\_QLOW} * K_R} + K_O \qquad (9)$$

KR and KO are empirically derived values that are initially set as $K_R = 1$, and $K_O = I_{Peak\text{-}Peak\text{-}Ripple} / 2$. We will discuss more about fine tuning these values in a following section titled Calibrating Your Design For Accurate Reporting In Software.

Considerations When Choosing a Low-Side MOSFET

The best case scenario when designing a sampling system is to choose an AFE that has a range that matches the expected signal range. In this case the AFE is already fixed. So it falls on the designer to choose a low side MOSFET that offers sufficient signal to best utilize the input range of the AFE while still considering the efficiency, size, and cost of the system. If telemetry is important, then please consider optimizing the low-side MOSFET to have sufficient RdsOn to give a clear signal across the expected load range. In the case of a low current system (i.e. less than approximately 5A where IFE_GAIN is going to be 8) consider MOSFETs that will be close to but less than the following formula:

$$R_{dsOn\_QLOW} \le \frac{120mV}{\left(I_{OUT} - \frac{1}{2} I_{Peak-Peak-Ripple}\right)} \qquad (10)$$

In the case of a higher current system (i.e. greater than approximately 10A where IFE_GAIN is going to be 4) consider MOSFETs that will be close to but less than the following formula:

$$R_{dsOn\_QLOW} \le \frac{280mV}{\left(I_{OUT} - \frac{1}{2} I_{Peak-Peak-Ripple}\right)} \qquad (11)$$

Obviously there is quite a bit of overlap where an IFE_GAIN setting of either 4 or 8 would be a satisfactory setting. The point is to pick a MOSFET that gives the best signal quality for the gain setting while also considering trade-offs of efficiency, size, and cost.

If some considerations are given significantly more emphasis, then the telemetry can be made to be ineffective for much more than over current protection. For example, in an extreme case where a 1mΩ MOSFET is used in a 4A system with 30% ripple, the difference between no load and full load would only be 2-3 bits out of 127. That is only a 1.5-2.3% usage of the AFE range.

CALIBRATING YOUR DESIGN FOR ACCURATE REPORTING IN SOFTWARE

Empirically Adjusting the Calibration Constants

For accurate current measurement utilizing embedded software that gathers data from the XRP7724 it is important for good engineering of the power stages.

Since the sense element for current measurement is a MOSFET there is a relatively high error present due to the coefficient of resistance versus temperature of the MOSFET R_{dsOn}. The good news is that the distribution curve of any particular MOSFET's R_{dsOn} over production quantities is very narrow. All of this means, that if you let your power solution run for a while and get up to its nominal operating temperature, then you can do accurate calibrations for the most likely operating temperature range.

The process is to collect some measurement data to establish a slope. Place a known load on the power stage at something like 20% and 80% of maximum design output current. This is $Iout_{min\text{-}meas}$ and $Iout_{max\text{-}meas}$. Next, read back the current measured by the XRP7724 using the process in the 'Interrogating the XRP772X for Telemetry' section and formulas (7) and (9) with K_R = 1 and K_O = 0.

This gives $Iout_{max\text{-}GUI}$ and $Iout_{min\text{-}GUI}$. Using the formula below you can determine the slope adjustment constant K_R to multiply your R_{dsOn} number by to match the measured slope. This is the first part of the calibration process.

$$K_R = \frac{(Iout_{max-meas} - Iout_{min-meas})}{(Iout_{max-GUI} - Iout_{min-GUI})} \qquad (12)$$

To demonstrate how different K_R values affect the results let's look at an example. Figure 3 shows plots of current over a load. These plots are calculated from a single set of current sense data from the XRP7724 using different values of K_R. The "Actual" plot is shown to display the applied load current for the measurements.

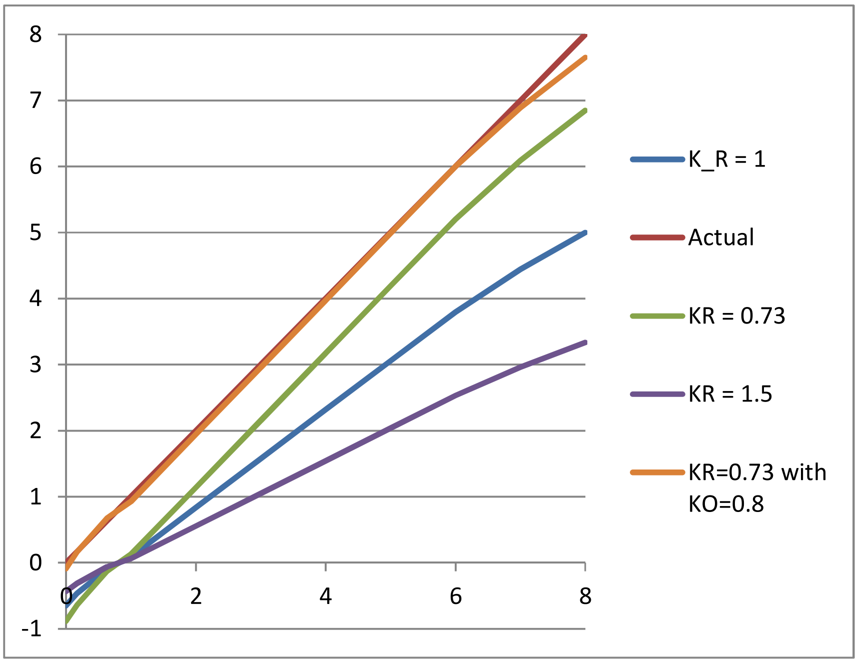

Figure 3 - Comparison of Single Data Set Displayed with Multiple K_R Values
X-Axis: Load Current (Amps); **Y-Axis**: Calculated Current (Amps) from Data

As you can see in the plots the data set for KR = 0.73 is tracking the slope of the "Actual" trace most precisely.

Once the K_R value is found, then an offset current value K_O should be determined.

From the plots in Figure 3, using a KR of 0.73, then an offset value of K_O = 0.8A is needed to zero the slope at the origin. This gives a strong calibration over the operating range of this particular 6A output power stage. This is the second step of the calibration process.

By following this empirical process it's possible to remove any explicit consideration of ripple current and duty cycle from the math by aggregating their impact into the constants K_R and K_O.

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Using PowerArchitect™ 5.1 to Interactively Set Calibration Constants

When using the Dashboard in PowerArchitect™ 5.1 or later there is a 'XRP7725 Telemetry' button that will bring up a new window for interactively calibrating values for KR and KO. The XRP7725 is unique in that the part records a sum of the current readings for the purpose of using equations (7) and (9) to derive an amp*sec measurement. These equations would need to be modified slightly to take into account the number of samples in the sum as can be seen in Figure 4. It should be noted that this method also improves accuracy by reducing quantization noise in the ADC by the square root of the number of samples. The instantaneous reading which is used to provide the datasheet accuracy limits includes that quantization noise. See the XRP7725 for more detail on this enhanced current measurement.

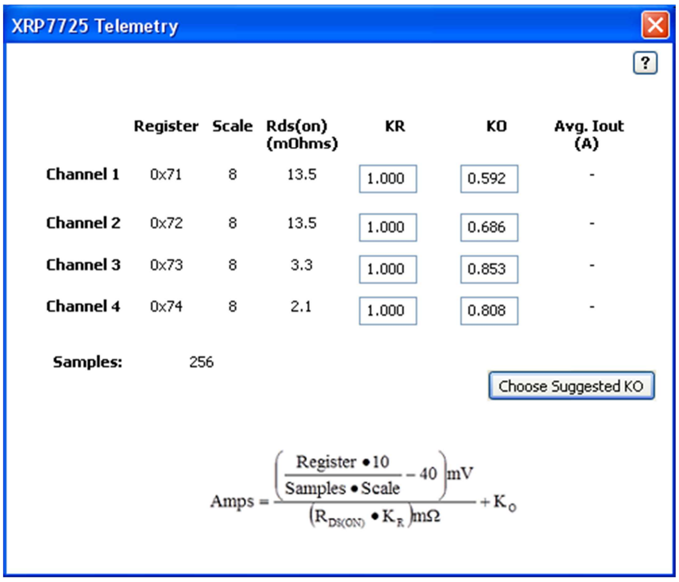

Figure 4 – Chip Telemetry Pop-Up Window

Future versions of PowerArchitect™ will include calibration inputs for instantaneous current measurement for other members of the XRP772X family. The most recent version of PowerArchitect™ can be downloaded from http://powerxr.exar.com/. Please review the release notes.

Special consideration when designing with wide input ranges

Systems with a very wide input voltage range such as Li+ battery stacks effect the duty cycle which changes the peak to peak ripple current. In systems like this, the empirical method of finding a constant 'K_R' that incorporates the MOSFET R_{dsOn} and $I_{Peak\text{-}Peak\text{-}Ripple}$ will be flawed across some of the operating range. In this case it is better when writing your own software to include a value for inductance 'L' for each channel and the necessary register reads to determine Vin, Vout, and Fsw. With this information it is easy to determine changes in ripple current and calibrate the results accordingly.

$$I_{Peak-Peak-Ripple} = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{(V_{IN} * F_{SW} * L)} \quad (13)$$

$$(V_{PGND} - V_{LX}) = \frac{(10mV * ADC\_OUTPUT)}{IFE\_GAIN} - 40mV \quad (14)$$

$$I_{OUT} = \frac{(V_{PGND} - V_{LX})}{R_{dsON\_QLOW} * K_R} + \frac{I_{Peak-Peak-Ripple}}{2} + K_O \quad (15)$$

$$I_{OUT} = \frac{(V_{PGND} - V_{LX})}{R_{dsON\_QLOW} * K_R} + K_O \quad (16)$$

The value for the inductor (L) should be a known constant. ANP-38 discusses the Automatic Programming Interface to the XRP7724. From this document we can learn the commands to find Vin and Vout.

- PWR_READ_VOLTAGE_CH0/1/2/3 (0x10, 0x11, 0x12, and 0x13) will give the Vout measurements for all 4 channels respectively with a scale of 15mV/bit.
- PWR_READ_VOLTAGE_VIN (0x14) will give the Vin measurement as sampled at the Vin pin of the XRP7724 with a scale of 12.5mV/bit.

The last parameter is switching frequency.

There are two components to calculating the switching frequency. First, there is the fundamental frequency. Second, there is the frequency tier (i.e. fundamental multiplier of 1x, 2x, 4x).

To determine the fundamental frequency read registers:

- 0xC40A (STA_COUNTER_RESTART_STATE_UPPER) Bits[0:1]
- 0xC40B (STA_COUNTER_RESTART_STATE_LOWER) Bits[0:7]
- 0xC40C (STA_FREQUENCY_TIER) Bits[7:0]

These first two registers comprise 10 bits that set a counter with the internal 103MHz clock. Use the formulas:

$$Count = (STA\_COUNTER\_RESTART\_STATE\_UPPER) \& 0x03 \bullet 2^8 + (STA\_COUNTER\_RESTART\_STATE\_LOWER) + 1 \quad (17)$$

$$F_{fundamental}(kHz) = 103000 / Count \quad (18)$$

The third register is for determining frequency tier. It is an 8 bit regiser with 2 bits per channel. The lowest two bits are channel 0. A value of b00 is 1x, b01 is 2x, and b11 is 4x.

Register Definition for 0xC40C (STA_FREQUENCY_TIER), b00 = 1x, b01 = 2x, b11 = 4x							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Channel 3		Channel 2		Channel 1		Channel 0	

To calculate F_{SW} for each channel multiply the fundamental frequency of the XRP7724 found in formula (18) by the frequency tier for each channel.

Discussion on Accuracy

Let's address the practical accuracy of the current sense. First, the ADC output bit length and range determines the resolution of the accuracy. In the Low Range (IFE_GAIN of 8) the accuracy is based on 1.25mV/LSB typically. At room temp the XRP7724 precision is +/-3 LSB (+/- 3.75mV). Over full temperature range the precision is +/- 8 LSB (+/- 12mV). In the High Range (IFE_GAIN of 4) the accuracy is based on 2.5mV/LSB typically. At room temp the precision is +/-2 LSB (+/- 5mV). Over full temperature range the precision is +/- 5 LSB (+/- 25mV).

Second, inductors are fairly rugged devices, but they are not entirely linear. Their inductance often decreases with ever increasing load currents depending on the inductor construction. As this inductance decreases, the peak to peak ripple current will increase.

In terms of the empirically fitted solution found using this document the offset current constant K_O will move off target at higher currents. Thus, this inductance swing will ultimately result in lower than expected current measurements at higher load currents. You can see this effect in Figure **3** in all the plots as they pass 6 Amp.

Third, MOSFETs such as Q_{LOW} have an R_{dsOn} value that varies with temperature at a rate of approximately 0.4%/C depending on process and manufacturer. This results in R_{dsOn} increasing in resistance with rises in temperature. This is problematic since the MOSFET is the sense element. To cope with this accurate calibration relies on the power stage being allowed to warm up to typical operating temperatures before this calibration process.

All of these errors together will stack up to affect accuracy so that the generally accepted best case measurement will be +/- 15%. Certainly more calibration and curve fitting can be done in software with more characterization of temperature operating points and inductor bias currents. The best case over production runs has been found to be +/- 10% in a controlled operating environment.

For more accurate current metering, a current sense amplifier with a precision current sense element can be used.

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	11/27/2013	Initial release of document
1.0.1	11/30/2013	Minor grammatical corrections

FOR FURTHER ASSISTANCE

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