

INTRODUCTION

The XRP77XX series family integrates Internal Gate Drivers for all 4 PWM channels. These drivers are optimized to drive both high-side and low side N-MOSFETs for synchronous operation.

Normally these drivers are required to be close to the MOSFETs they are driving due to their high current and high speed rise and fall times.

In many Applications there will be a need to place one or more rails in a Power XR application at some distance from the controller. This Application note will introduce and examine from both a theoretical and practical standpoint a layout design technique that will allow the MOSFETs to be as much as 6" (152mm) from the driver.

THEORY

As discussed in ANP-32 the routing of the drive signals from the Power^{XR} controller with its integral drivers to the power stage MOSFETs has to be carefully considered. When the MOSFETs are moved away from the driver (more than 20mm) the parasitic parameters of the layout can become dominate resulting in inadequate performance of the power system.

In order to eliminate these parasitic issues Exar has developed a layout approach that allow the power stage to be as much as 150 mm distant and still work as expected.

The basis of the operating theory is that the drive to the MOSFETs is a pulse of current and that if one views the drive lines (conductors) as a pulse transmission line with a capacitive termination (gate and Miller capacitance) then the parasitics can be overcome.

Figure1 below shows a transmission line design that has been created to match the drive capability of a 3 ohm drive stage such as can be found in a XRP7714.

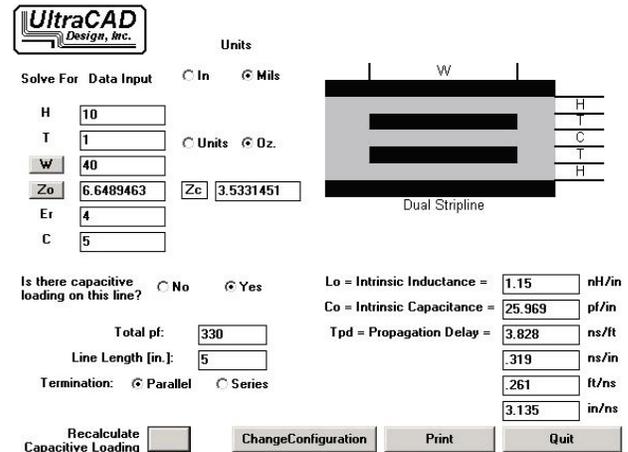


Figure 1.

Formulas:

$$Z_o = \frac{\left(\frac{80}{\sqrt{E_r}}\right) \times \ln(1.9((2H)+T))}{((0.8W)+T)} \times \left(1 - \left(\frac{H}{4(H+C+T)}\right)\right)$$

$$L_o = 0.001(C_o \sqrt{Z_o})$$

$$C_o = (2.82 \times E_r) \frac{(0.268 \times W) + (0.335 \times T)}{\ln(2 \times (H - T))}$$

$$T_{pd} = 0.0833(1.016\sqrt{E_r})$$

Modifying for Capacitive Load:

$$k_{parallel} = \sqrt{1 + \frac{C_d}{C_o}} \quad Z_c = \frac{Z_o}{k} \quad T'_{pd} = T_{pd}k$$

We are using a design tool from http://www.ultracad.com/diff_calc.htm to analyze our transmission line construction.

While other possibilities exist for a transmission line design, such as microstrip, stripline and embedded microstrip, a dual stripline, also called a broadside coupled stripline, was chosen in order to have the magnetic field produced from the current pulse that charges and discharges the MOSFET capacitance be cancelled by the proximity effect of the opposing currents. This lowers the Z of the Dual stripline ~66% vs. stripline. In addition radiated noise is lowered.

In the four layers shown in Figure 1 we use the top and bottom (full width black area) conductor as a power plane or ground. From an AC perspective both can be considered ground. The two inner conductors are the gate and source leads to the MOSFET. These signals come from the internal driver of the XRP77XX from the drive pins. These pins are designated as in this example for channel 1 of the XRP7714:GL1 is the Gate, low side MOSFET and the return path from the MOSFET source is PGND1, power ground 1.

Here are some basic guidelines for the design of a broadside coupled stripline: (See Fig.1)

1. Close traces, the "C" dimension lowers the Z. Greater spacing increases Z.
2. Increasing W will decrease Z by about 0.5Ω per 20 mils

3. Increasing copper thickness (weight) for each oz. of weight or .4 mils the Z will rise by 4 ohms.
4. Increasing length will not change Z but will increase the amount of parasitic capacitance that the driver will see. In our example it is about 26pF per inch. This will add to the losses in the driver.
5. Designs can accommodate some discontinuities (e.g. vias, unequal traces) to allow for getting a layout routed. These runs are not as critical as many digital signals.
6. Er is set to 4, rather than 4.7, as the 5 mil prepreg, style 2116, has a lower dielectric constant than standard FR-4.

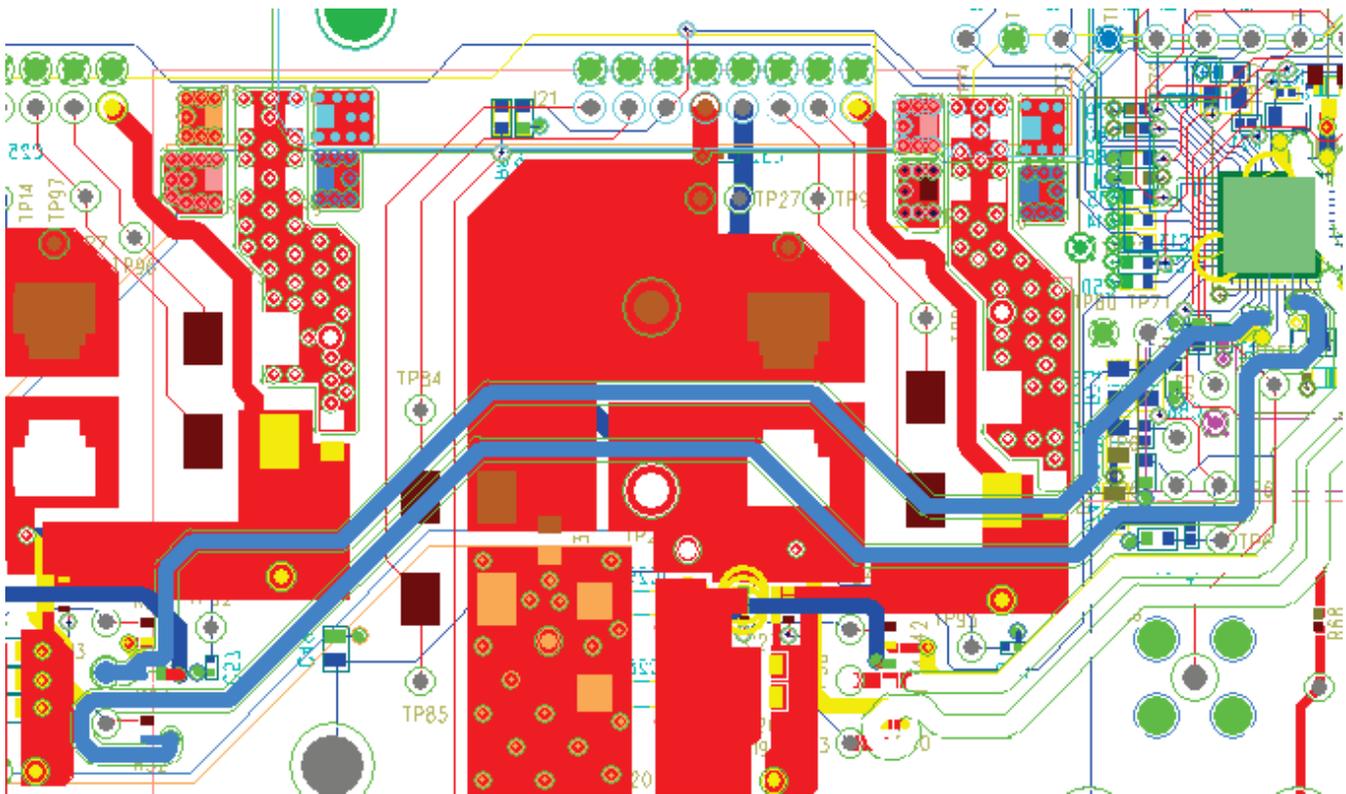


Figure 2. Gate Conductors in Experimental Board shown in Blue on layer 3.



Figure 3. Power Ground and LX signal conductors shown in blue on layer 4.

In Figure 1 notice that the L_o is very low due to cancelling fields but the C_o is relatively high. In our case the additional 125pF will result in $0.5 \cdot 125 \times 10^{-6} \cdot 5^2 \cdot 2 \cdot 500K$ or about 780uW of additional power loss in the drive circuit at 500KHz.

The evaluation of how well this technique works is a simple one. By viewing the rise and fall time of the phase node on each regulator we can see how well the MOSFETs have been driven. Below are examples of the waveforms observed in our experimental board and in some other synchronous converters.

SCHEMATIC

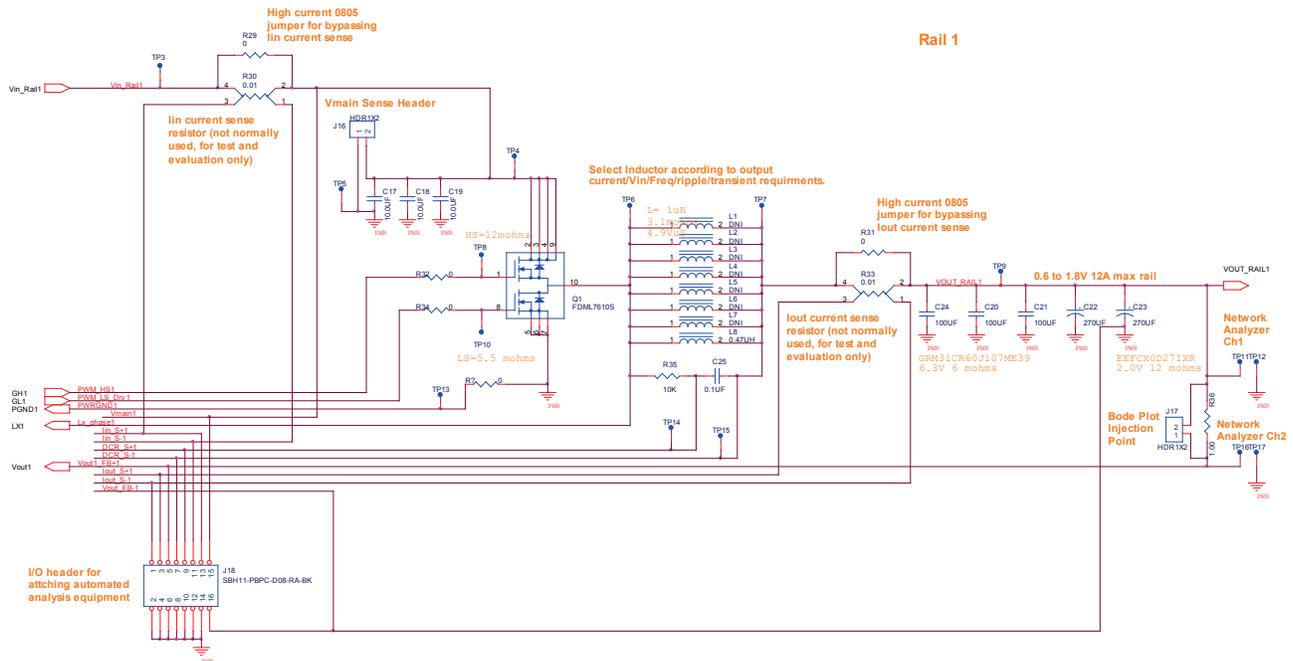


Figure 3: Schematic of Experimental Board

**WAVEFORMS****MEASUREMENT DISCUSSION**

Channels 1 and 4 are set for a 250MHz bandwidth and deskewed for time and calibrated for magnitude (the reason CH3 is set at 19.2mV/div) while Ch3 is a 100MHz bandwidth and is also deskewed for time. The high side gate waveform is measured between the source (Lx node on the XRP7714) and the gate of the MOSFET directly at the pins of the MOSFET using a differential probe. The phase node (Lx) waveform is measured directly at

the lower MOSFET with the ground reference tied at the lower MOSFET source. The lower MOSFET waveform is measured directly at the gate of the MOSFET with the ground reference tied at the lower MOSFET source.

On the following pages are some examples of other converters phase nodes. In this example a 12V input, 3.3V output, at 12A converter is shown that uses a DrMOS type power stage. The gate driver is completely optimized for the particular MOSFETs being used since all devices are on the same silicon.

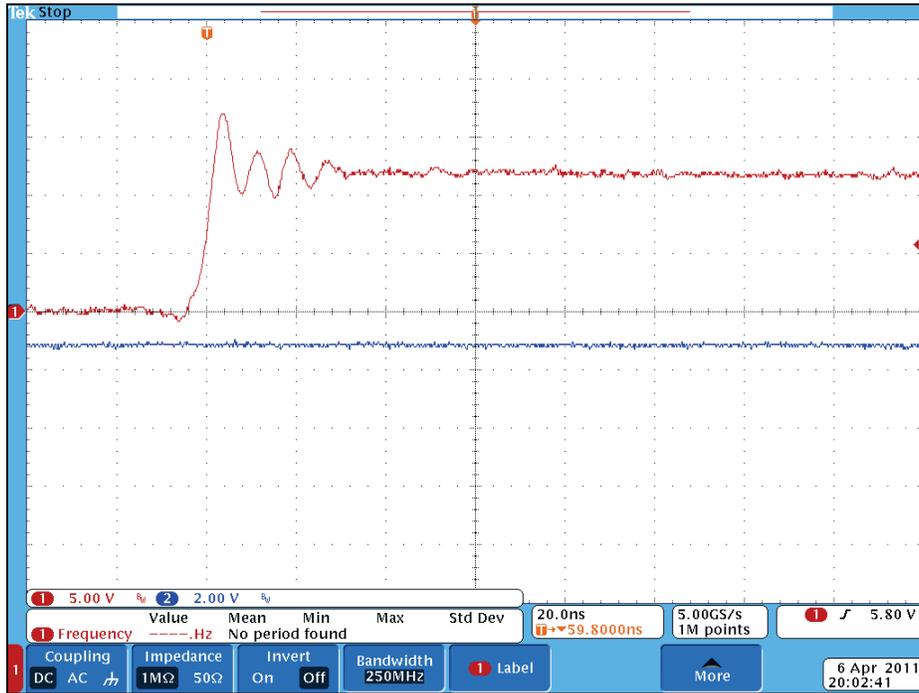


Figure 4: Rising Edge DrMOS Power stage phase node (no snubber)

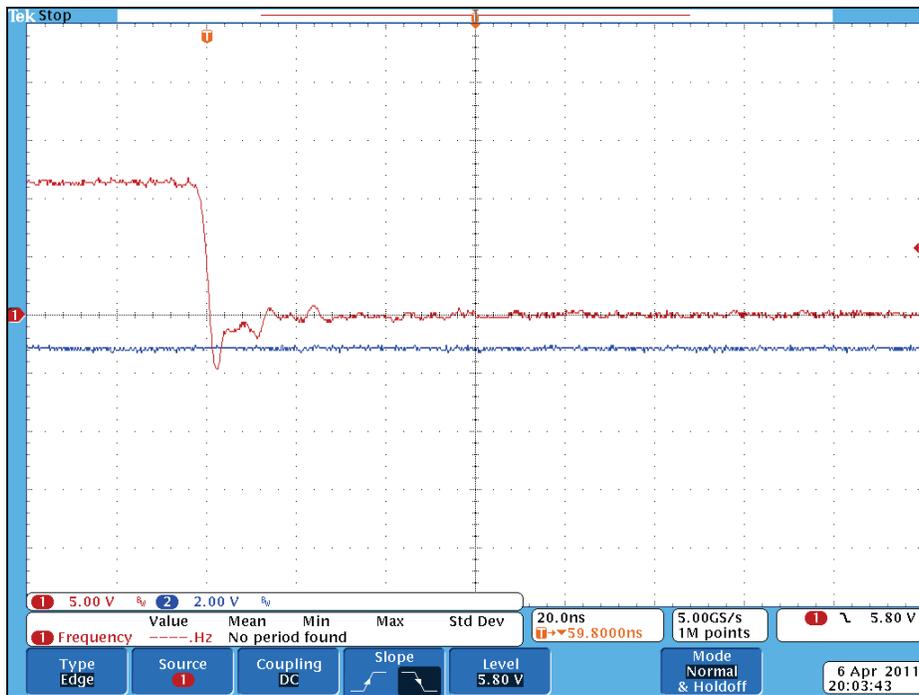


Figure 5: Falling Edge DrMOS Power Stage phase Node (no snubber)

Here is an example of a discrete MOSFET (QFN) power stage with 12A 1V output in two phases with a snubber in place.

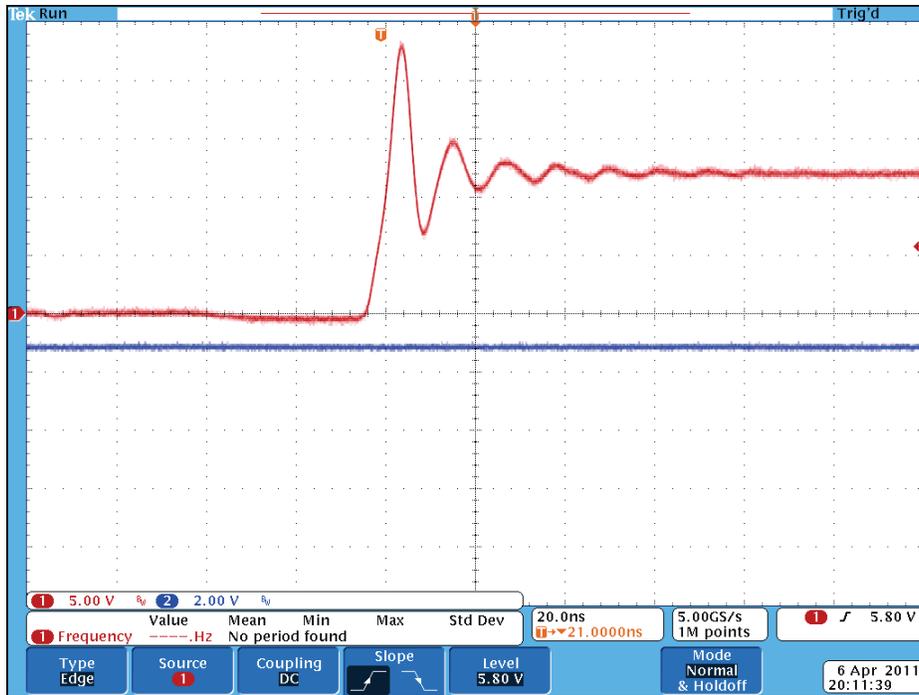


Figure 6: Rising edge Discrete MOSFET phase Node (with snubber)

(notice the level of the ringing is much greater than on the DrMOS power stage due to less parasitic elements)

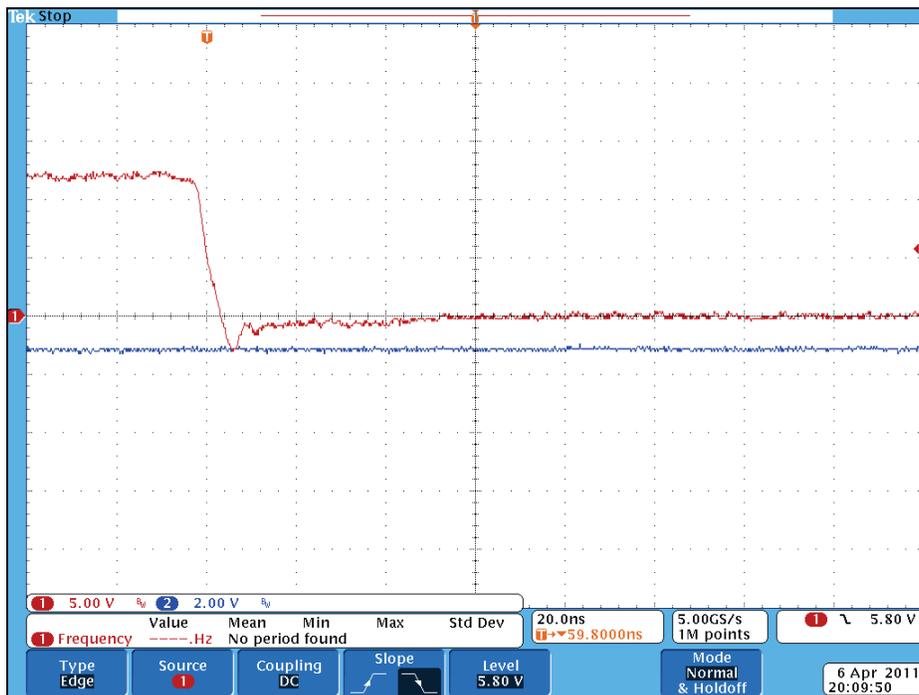


Figure 7: Falling Edge Discrete MOSFET phase Node (with snubber)

Now let's look at the performance of the experimental board.

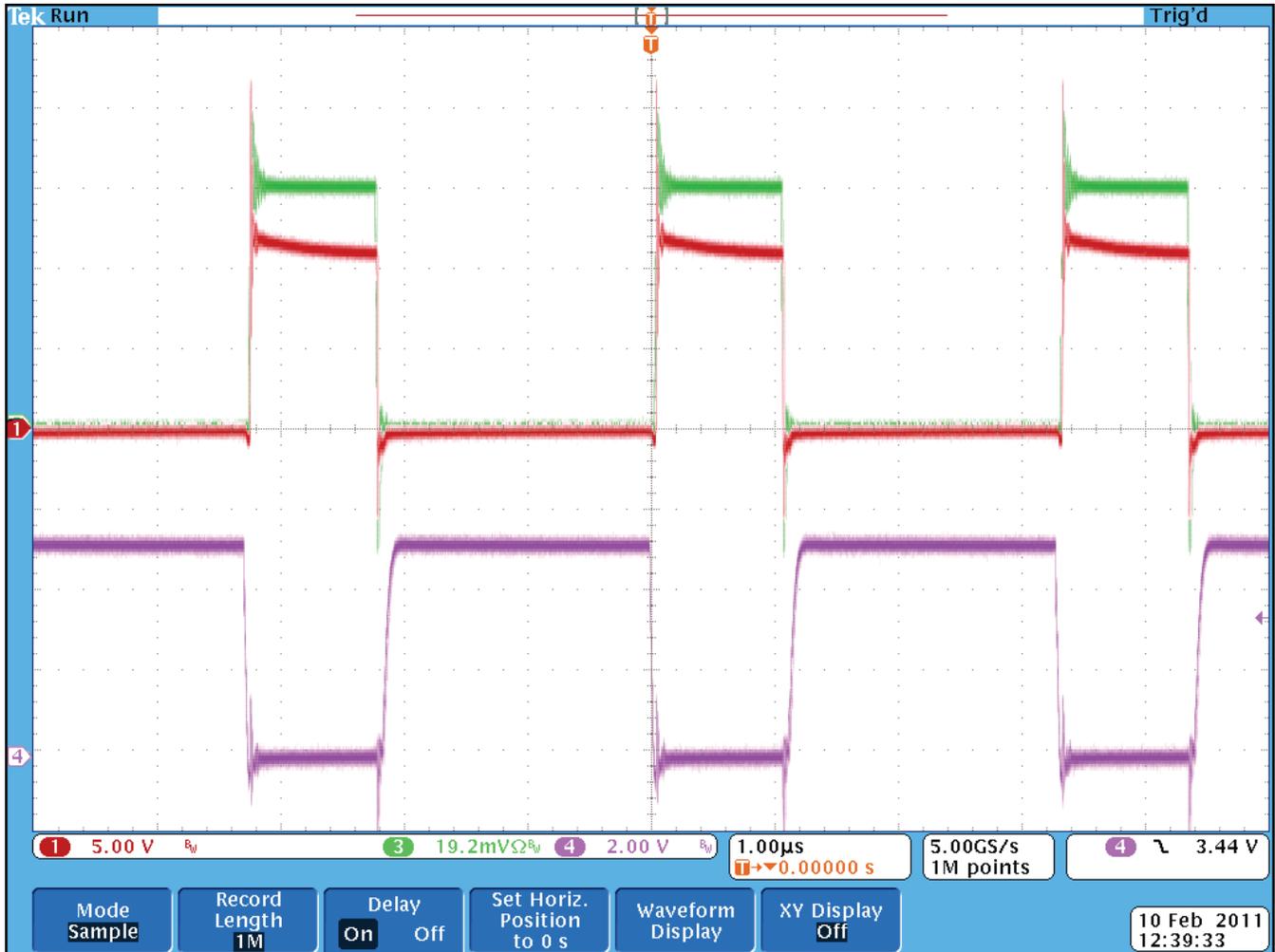


Figure 10: Over all operation at 12V input, 3.3V output and 12A load. Inductor is as shown on the schematic previously. Ch 3 (green) is high side drive at 2V/div, Ch4 (magenta) is low side drive at 2V/div. Ch1 (red) is the phase node at 5V/div. Package is a dual MOSFET 3mm x 4.5mm QFN. No snubber is used.

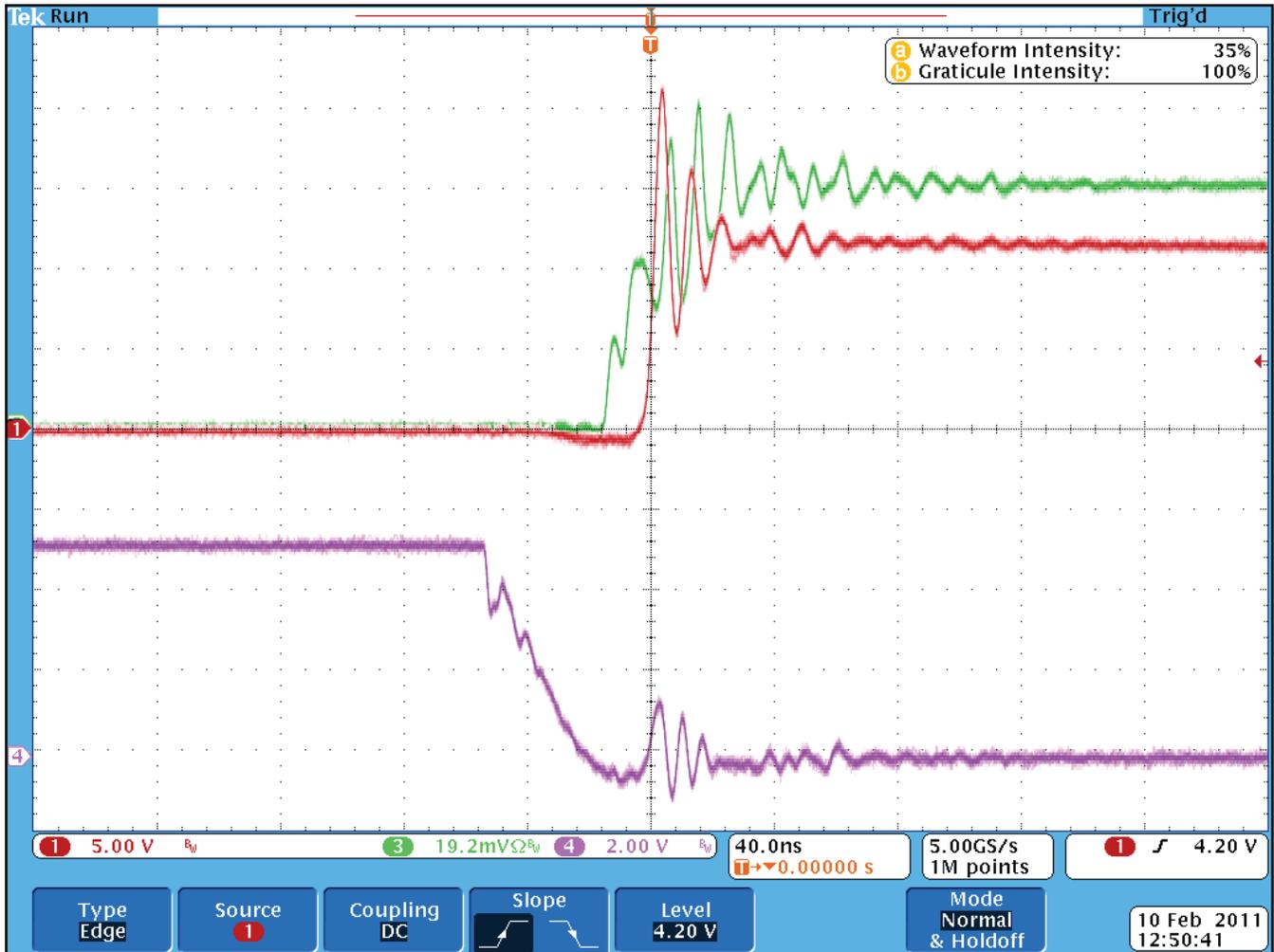


Figure 11: Rising edge drive (phase node). Ch 3 (green) is high side drive at 2V/div, Ch4 (Magenta) is low side drive at 2V/div. Ch1 (red) is the phase node at 5V/div.



Figure 12: Detailed close up of rising edge showing phase node rise time. Ch 3 (green) is high side drive at 2V/div, Ch4 (magenta) is low side drive at 2V/div. Ch1 (red) is the phase node at 5V/div. Note that the low side drive has a low enough Z to keep the gate voltage below 1.8V during the phase node rise time even though the MOSFET is over 5 inches away from the driver.

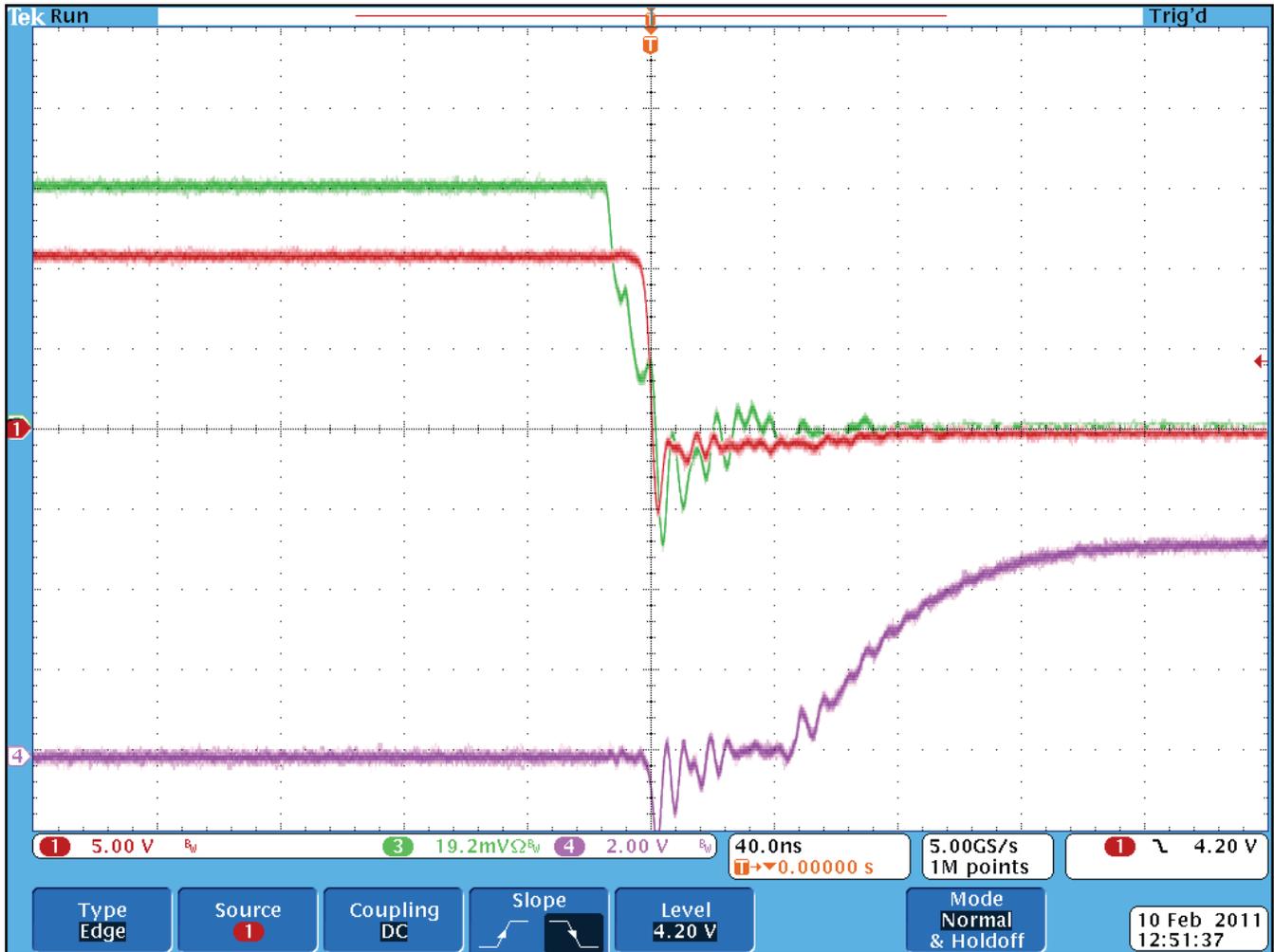


Figure 13: Falling edge drive (phase node). Ch 3 (green) is high side drive at 2V/div, Ch4 (magenta) is low side drive at 2V/div. Ch1 (red) is the phase node at 5V/div.

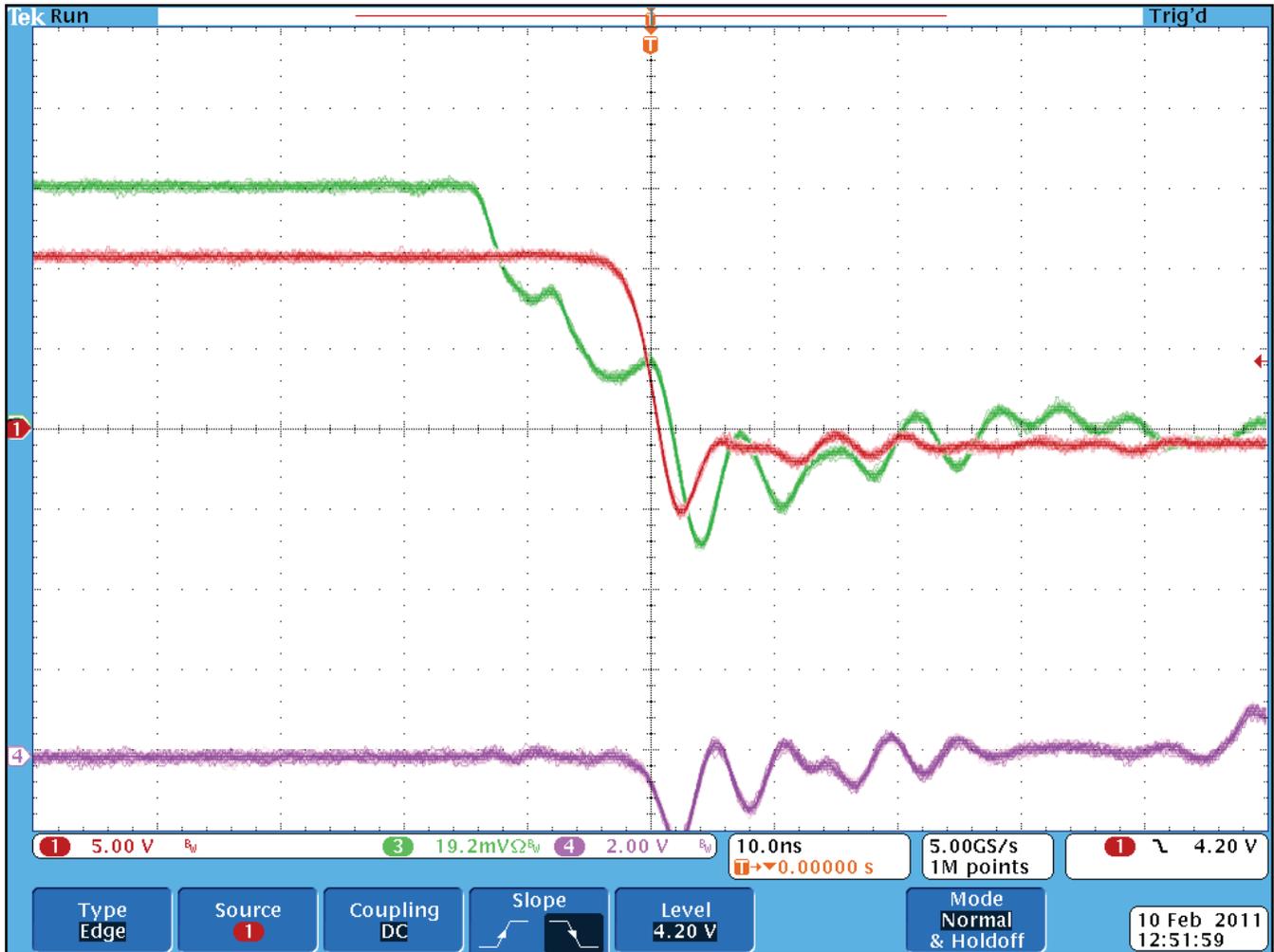


Figure 14: Detailed close up of falling edge showing phase node fall time. Ch 3 (green) is high side drive at 2V/div, Ch4 (magenta) is low side drive at 2V/div. Ch1 (red) is the phase node at 5V/div.

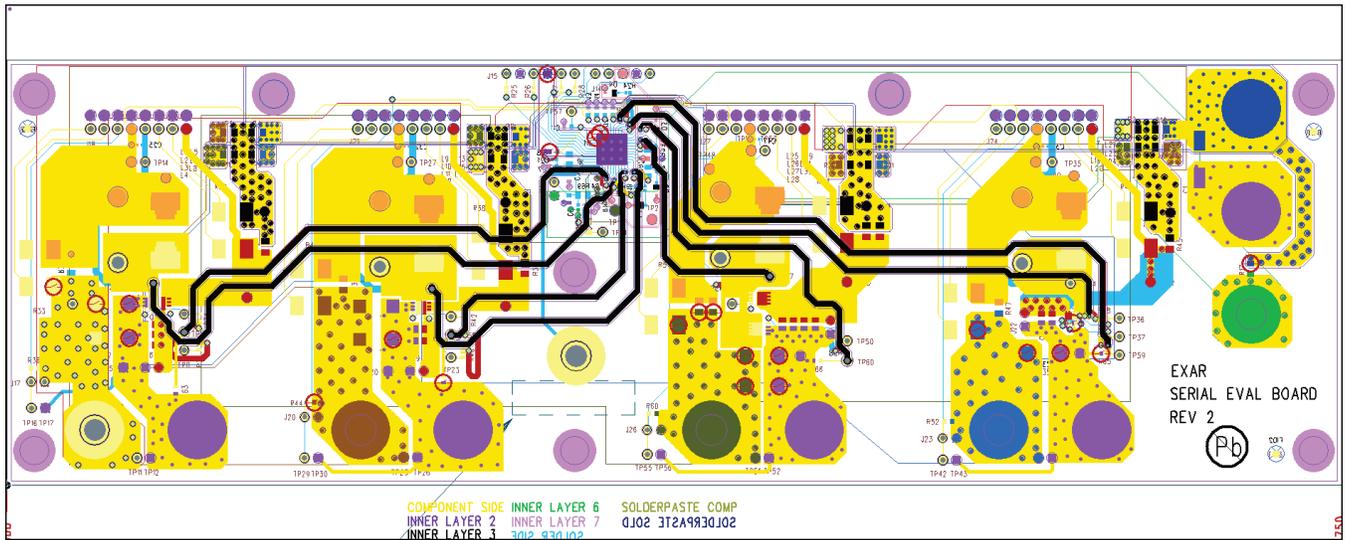


Figure 15: Layout showing routing of traces in black (the output on the left side is the one under test). All four switching outputs of the 7714 are shown.

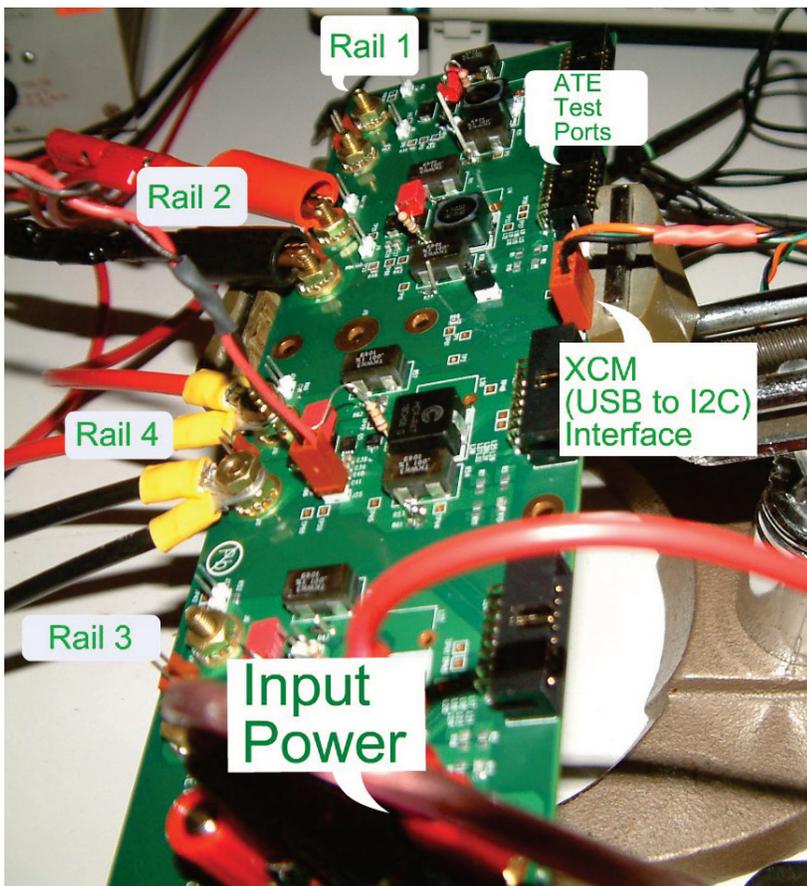


Figure 16: Experimental Board Test Set up

RESULTS

Analysis of the results will concentrate primarily on the behavior of the phase node. Whilst it could be argued that any changes are best observed at the gate drive signals, it's the impact to the DC/DC performance as a whole we are concerned with here. Since the gate signals main function is to establish the correct behavior of the phase node then this will be used as the primary metric. Any anomalies in this signal will negatively impact the efficiency, ripple and jitter of the converter.

The key elements of the phase node waveform to consider in determining its validity are the rise and fall times and to a lesser extent the ringing. Comparing the measurements made with the power FETs at a distance of 5" from the controller based gate drivers (indicated by the red trace in Figures 11 (rising) and 13 (falling)) and those from the plots obtained of a similar arrangement with short gate traces (Figures 6 (rising) and figure 7 (falling)) it can be seen that the rise times are virtually equal at 6ns. This relationship holds too for the fall times which both read 5ns.

The results for the ringing also bear a close resemblance, with both showing 100% overshoot and a duration of approximately 50ns.

Lastly as a way of indicating what can be achieved when PCB layout is taken out of the gate drive equation, consider the plots found in Figures 4 and 5. These indicate the phase node behavior on a drive train utilizing a DrMOS based power train. This represents the ultimate in Gate drive to FET coupling as both functions reside on the same device. As such it can be considered as the reference standard for gate drive circuitry.

Examining these plots reveals a rise time of 5ns and a fall time of 4ns. In addition, the ringing measures as 45% overshoot with a

duration of 40ns. The reduced ringing in this case is attributable to the lower parasitics associated with close coupling of the gate drivers and power FETs.

It can thus be seen that phase node performance has not been degraded at all by using the longer gate drive traces, and furthermore that this technique even compares reasonably well to the optimal integrated drivers on the DrMOS set up.

Lastly measurement was also made of the gate drive signals for the extended trace solution. This was to verify that the distance hasn't prevented the gate driver from exerting proper control over the gate at the point of phase node current commutation. It can be seen from Figures 12 and 14 that the low side gate remains considerably lower than 1.8V when both the high to low and low to high transitions of the phase node occur, ensuring cross conduction cannot occur.

CONCLUSION

Correct layout is always a vital part of any good switch mode converter design. Experience dictates that adding any additional distance between the gate drivers and power FETs in such a design would be a violation of those principles. However this app note has shown that when attention is paid to the traces between gate drivers and the FETs, and a few simple guidelines adhered to, a distance of up to 6" is achievable with virtually no impact on the overall performance of the converter. This in turn allows designers to take full advantage of the higher level of integration offered by the XRP77xx series of digital multi channel controllers without having to sacrifice the geographic flexibility afforded by individual POL solutions.



DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	05/02/2011	Initial release of document

FOR FURTHER ASSISTANCE

Email: customersupport@exar.com
Exar Technical Documentation: <http://www.exar.com/TechDoc/default.aspx?>

EXAR CORPORATION

HEADQUARTERS AND SALES OFFICES

48720 Kato Road
Fremont, CA 94538 – USA
Tel.: +1 (510) 668-7000
Fax: +1 (510) 668-7030
www.exar.com



NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.